Copper Electroplating for Advanced Interconnect Technology

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Copper electroplating for gap fill of damascene structures on advanced interconnects has been demonstrated to be a viable technology. Development and optimization of robust electroplating processes for void-free fill requires a full understanding of the role of the plating solution components (brighteners, levelers, and suppressing agents) and their behavior as a function of plating amperage, waveform and bath temperature. Methodology for void-free fill of damascene structures will be presented, as well as an interpretation of grain growth transformations and morphological changes for the thin copper films.

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Introduction

The Semiconductor Industry is moving towards the implementation of electroplated copper for metallization of advanced interconnects. Motorola and IBM will have commercial products utilizing this metallization scheme for sale in 1999. Full integration of electroplated copper into the chip manufacturing process will require the optimization and control of a number of key issues, i.e., plating bath composition, bath additives, and deposition parameters. Additionally, a thorough knowledge of copper thin film morphology must be developed. Table 1 presents the National Technology Roadmap forecast for insertion of the various technology nodes (critical dimension of trenches).[1]

Table 1
Insertion Node for Interconnect Technology

Year	Critical Dimension
1997	250 nm
1998	180 nm
2001	150 nm
2003	130 nm
2006	100 nm

For copper electroplating to be extendible to the smaller feature sizes, 0.25µm (9.75µ-in) to 0.10µm (3.9µ-in), technology improvements become important not only for electroplating but for photolithography, etch, barrier and seed, and post plating chemical-mechanical polishing (CMP).

Presently, copper electroplating of interconnects is performed using a commercially available sulfuric acid cupric sulfate solution utilizing proprietary additives similar to that used for the printed wire board process. Table 2 lists a typical composition for a copper plating solution used in the semiconductor manufacturing process.

Table 2
Composition of Copper Electroplating Bath

Component	Concentration
Cu (as metal)	15-19 g/L
H_2SO_4	150-225 g/L
Chloride ion	50-90 mg/L
Additives	variable
Parameter	**Operating condition**
Temperature	21-27°C (70-80°F)
Current Density	4.5-22 mA/cm^2 (5-20 ASF)
Anode	Soluble or insoluble

These solutions have demonstrated satisfactory electroplating fill for feature sizes down to ~0.20 µm (7.8 µ-in) with an aspect ratio (AR) of 4 (ratio of feature depth-to-width). Seam voids within the trenches and vias begin to appear during electroplating of features smaller than 0.20 µm (7.8 µ-in) and are partially related to the inability of the additive system to function properly in this regime. In contrast to plating of the through holes in the printed wire boards, the plating of semiconductor devices requires filling of sub micron blind vias and trenches. The small feature size and hydrodynamic conditions present for wafer plating dictate that a specifically optimized plating chemistry and bath additive package be developed for this application. Currently, a great deal of research and development is on-going at semiconductor facilities, universities, tooling suppliers, and chemical suppliers to develop new chemistries and to fully understand the electroplating deposition kinetics of the semiconductor interconnects. Ultimately, semiconductor grade copper plating solutions will be available with additives tailored to provide true leveling for void free fill of interconnects.

Procedure

Presently, copper electroplating for semiconductor applications takes place typically on 200 mm (8 in) silicon wafers with plans to eventually shift processing to 300 mm (12 in) silicon wafers. Electroplating is performed in fully automated single wafer platforms designed for high volume manufacturing. Throughput for these tools is 10-12 wafers per hour per plating chamber, with most tools having 3-6 plating chambers. The plating process is designed to fill the features and provide sufficient overplate to achieve a high degree of leveling across the wafer. A post plating CMP process removes the copper overburden and prepares the wafer for the next layer processing. Multi-layer processing can have 6-9 layers of copper interconnects. Table 3 shows the processing steps required for single layer processing.

Table 3.
Wafer Process Flow

1. Dielectric Deposition
2. Lithography
3. Etch
4. Barrier and Seed Deposition
5. Copper Electroplating
6. CMP

Results and Discussion

Electroplating Fill Defect Mechanisms

Electroplating defects are manifested as either vertical seams or voids in the trenches or vias. Seams are associated with a pinching off of the opening prior to fill of the structure. Voids are associated with poor step coverage of the copper seed layer.

Collimated physical vapor deposition (PVD) was used to deposit 250 Å Ta barrier and 1000 Å Cu seed on the wafers. Collimated PVD Cu deposition is an inherently non-uniform process that provides a step coverage of ~5-8 %. Ideally, a minimum of ~100 Å of Cu seed on the trench lower sidewalls is sufficient for void free electroplating fill. Depositing 1000 Å of Cu seed provides ~50-80 Å of Cu seed on the lower sidewall of a 0.25 µm (9.75 µ-in) trench. The deposition of an excessive amount of copper seed at the feature opening can lead to a breadloafing effect, creating a re-entrant profile. Subsequent electroplating leads to seam voids. Figure 1 diagrams the fill sequence for the conformal fill of a re-entrant profile. Re-entrant etch profiles in the dielectric film will also lead to the formation of seams during electroplating .

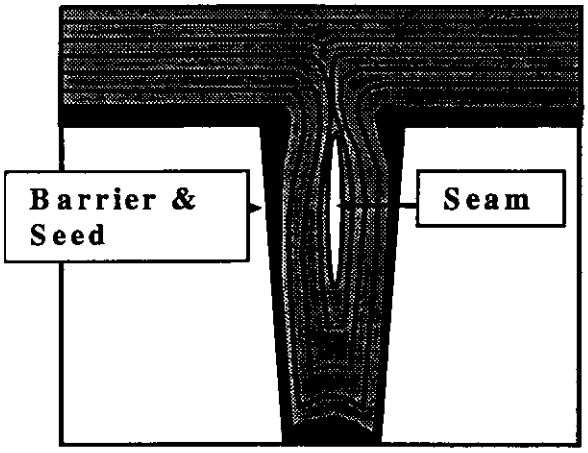
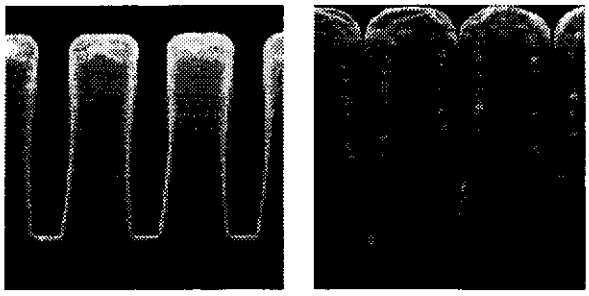


Figure 1 - Diagram of seam formation during conformal electroplating fill of re-entrant trench.

The SEM cross sections in Figure 2 show a partial fill of 0.25 µm (9.75 µ-in) re-entrant trenches. Examination of the PVD Ta barrier and Cu seed layer (SEM 1) reveals a re-entrant profile that leads to seam formation. SEM 2 shows that after 10 seconds of plating a seam is formed and that the fill mechanism is clearly conformal, i.e., the deposition rate at the trench top is essentially equal to that at the sidewall. Under these conditions there is little chance that the plating fill will be seam free.



(SEM 1) (SEM 2)

Figure 2 - SEM cross section of 0.25 µm (9.75 µ-in) trench AR 4, showing seam formation during plating timed sequence; SEM 1 is after barrier & seed deposition and SEM 2 is after 10 seconds plating.

Voids are associated with insufficient bottom sidewall coverage by the PVD Cu seed. Thin (<50Å) coverage on the bottom sidewall can result in the dissolution of the Cu seed layer by the corrosive nature of the sulfuric acid copper plating solution during initial immersion of wafer. Voids are more likely to occur during electroplating as the aspect ratio becomes large (AR >6) and step coverage is minimal. Figure 3 shows the formation of voids near the trench bottom where the step coverage by the collimated PDV Cu seed was insufficient for electroplating. Use of hot entry or minimal solution exposure (solution dwell time) of the Cu seed prior to initiation of the deposition process can minimize the formation of voids.

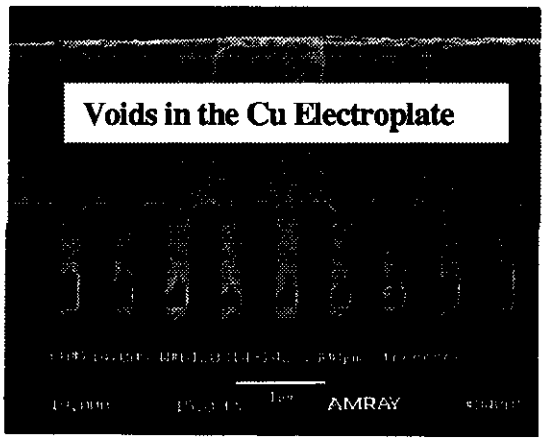


Figure 3 - Void formation as a result of thin PVD Cu seed layer on 0.25µm (9.75 µ-in), AR 6 trench sidewall.

The electroplated fill quality is effected by the operating temperature of the plating bath.[2] Figure 4 shows the copper fill of trenches over a temperature range from 15 - 35° C. Optimum fill was obtained at 20° C. Low temperatures cause the reduction in the mobility of the additive components thereby rendering them less effective. At temperatures of 30° C and higher the additives may be thermally degraded and lose their functionality, resulting in the formation of seams.

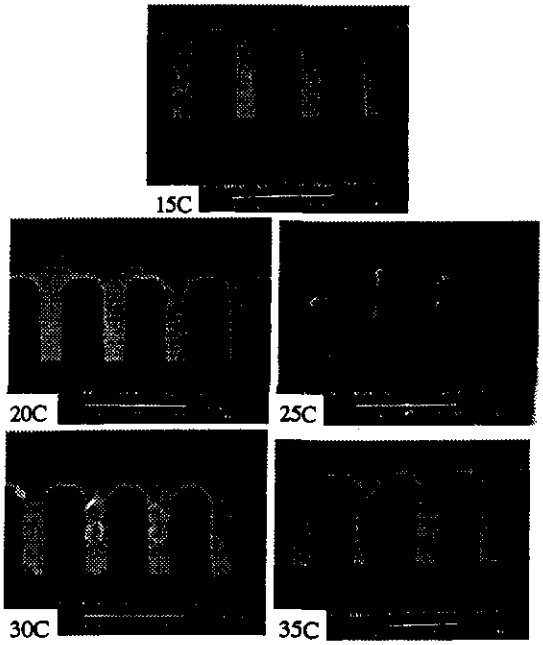


Figure 4 - Copper electroplating fill of 0.25 µm (9.75 µ-in) trenches, AR 4 at various temperatures.

Optimized Fill

Control of the plating current density and additive levels in the bath has a dramatic effect on the fill mechanism. Figure 5 shows a series of partial fills of 1 µ (39 µ-in) trenches that have been plated at 22 mA/cm^2 (20 A/ft^2) for 20 seconds, with varying additive levels. Clearly a higher concentration of leveling agent (top row SEM's) favored the formation of a bottom up fill mechanism. While increased suppressing agents lead to a diminished degree of bottom up fill. In all cases strong suppression or blocking of the deposition at the upper trench corners is apparent and is a necessary condition for void free bottom up fill. Figure 6 shows the cross section for a copper plated dual damascene structure with a 0.25µm (9.75 µ-in) via. The fill sequence for this structure consisted of a two step fill process; Metal 1 (M1) was electroplated first, then Via 1/Metal2 (V1/M2) were electroplated in one step after appropriate processing of M1 through CMP, lithography, and etch.

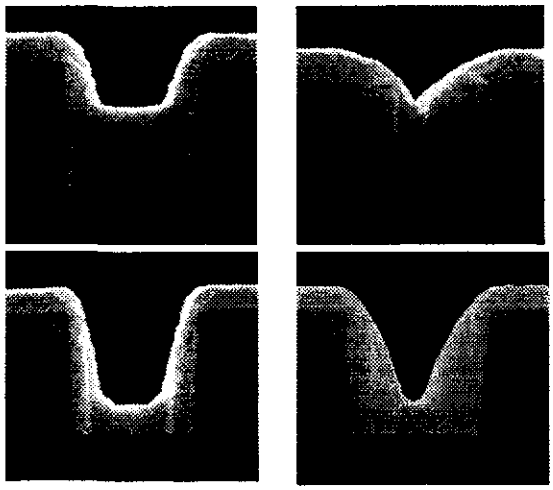


Figure 5- Partial fill sequence of 1 µm (39 µ-in) trenches for varying additive levels, deposited at 22 mA/cm^2 (20A/ft^2) for 20 seconds, top row: increased leveling agent, bottom row: increased suppressing agent.

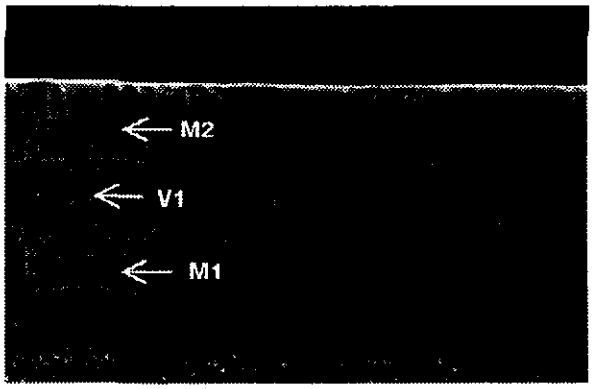


Figure 6 - Dual damascene fill: M1 (metal 1 layer), V1(via 1), M2(metal 2 layer).

While copper deposited in the absence of additives will be columnar in structure and contain large grains, deposition in the presence of additives produces an equiaxed-fine-grained deposit. The additives used for copper electroplating are generally organic compounds that act as inhibitors, grain refiners, ductilizers and may be co-deposited with copper. Key components in most additive packages used for copper electroplating include the following,

- **Brighteners:** These are generally organic compounds that contain sulfur and may also incorporate other functional groups. Examples include, thiourea and derivatives of thiourea, 4,5-*dithiaoctane-1,8,-disulphonicacid*,mercapto-propane sulfonic acid.[3] Brighteners are responsible for the formation of small grained, bright deposits.

They function by preventing the deposition of copper at preferred locations by enhancing the formation of new nuclei as opposed to the buildup of existing nuclei.

- **Levelers:** Effective levelers tend to be medium molecular weight organic compounds containing key functional groups, they have a low solubility in the plating solution, and have a low coefficient of diffusion. They act through selective adsorption on readily accessible surfaces, i.e., flat field areas and protruding high points. The mechanism of leveling has been postulated elsewhere and numerous models have been developed to explain their mechanism, but it is generally accepted that true leveling is a result of diffusion control of the leveling species.[4-5] Examples of leveling agents include but are not limited to poly amines such as derivatives of safronic dyes with and without an OH functional group attached. Additives that function as brighteners and suppressers may also impart a slight measure of leveling to the deposit. [6]

- **Suppressing Agents:** The characteristic of this additive component is the formation of a continuous film on the surface, which can completely block the electrodeposition of copper. Suppressing agents adsorb onto the wafer surface forming a diffusion layer which limits the transfer of brighteners and levelers into the features, promoting their adsorption at the feature opening, resulting in true leveling. In the presence of chloride ions the degree of adsorption and inhibition is further enhanced.[7] Suppressing agents include poly glycols such as polyethylene glycol, polypropylene glycol, co-polymers of polyglycols.[8-9] Suppressing agents are characterized by their high molecular weights, low solubility, and low coefficient of diffusion. The effectiveness of the suppressing agents is a function of the molecular weight of the polymer and must be tailored to the specific application.

Used alone these additives have a minimal effect on the leveling of the deposit, however formulated together they impart a synergistic effect that maximizes the leveling effects.

Morphology of Electroplated Copper

It has been experimentally determined that a 1.5 µm (58.5 µ-in) electroplated copper film will self anneal at room temperature in less than 50 hours.[10] Figure 7 shows the change in the resistivity of the copper film with time. The as deposited bulk resistivity of electroplated Cu is ~ 2.22 µOhm-cm and stabilized at 1.80 µOhm-cm approximately 50 hours later, a reduction of ~20%.

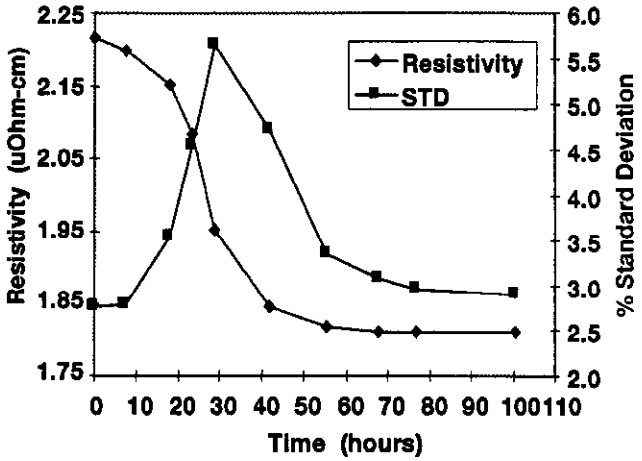


Figure 7 - Self annealing effect on resistivity and standard deviation.

Associated with the change in resistivity was a transition in the non-uniformity (% Standard Deviation) of the copper film from an initial value of ~3% one sigma to a maximum of ~5.5% one sigma during the midpoint of the self annealing process and finally returning to ~3% one sigma. Figure 8 shows that the stress transitions from compressive to tensile. Figure 9 shows the CMP polishing rates for the copper films at various times after electrodeposition. There is an overall increase of 35% in the metal removal rate for the self annealed copper attributed to a softening of the deposit with time (~ 40% reduction in hardness).

The observed transformations in the electroplated 1.5µm (58.5 µ-in) copper film are associated with the thermodynamic instability of the electroplated Cu film. The Cu film releases excess free energy through a complex process of recovery and recrystallization.[11] This transformation follows the Arrhenius equation,[12]

$$k = Ae^{-Ea/RT} \qquad (1)$$

Where k is the rate constant, A is a constant, E is the activation energy, R is the universal gas constant and T is the temperature. Copper electroplated at mid-to-high current densities, 13-22 mA/cm^2 (11.8-20 A/ft^2), in the presence of additives results in the formation of small-equiaxed grains containing a high density of defects. Increasing defect density increases the free energy leading to a lowering of the activation energy required for recovery and recrystallization. As a result the observed morphological transformations for the

1.5 μm (58.5 μ-in) copper film occurs at relatively low temperatures and times. The free energy is released through grain boundary annihilation. The final result is the transformation from small grains to large grains, reducing the number of grain boundaries, and therefore improving the conductivity of the deposit. A softer deposit after self annealing results in an overall improvement in the CMP metals removal rate. The grain growth is apparent in Figure 10 which shows the as deposited and self annealed copper on a blanket wafer. The grain size ranges from ~0.1μm (3.9 μ-in) for the as deposited film to >1.0μm (39 μ-in) for the self annealed film. Figure 11 shows the grain growth within a trench after a 120° C anneal. During the self anneal process the stress transitions from compressive to tensile. The annihilation of the small grains and the formation of large grains results in a net decrease in the deposit volume which creates a tensile stress. Figure 12 shows the effects on the film stabilization by thermal annealing at various temperatures.

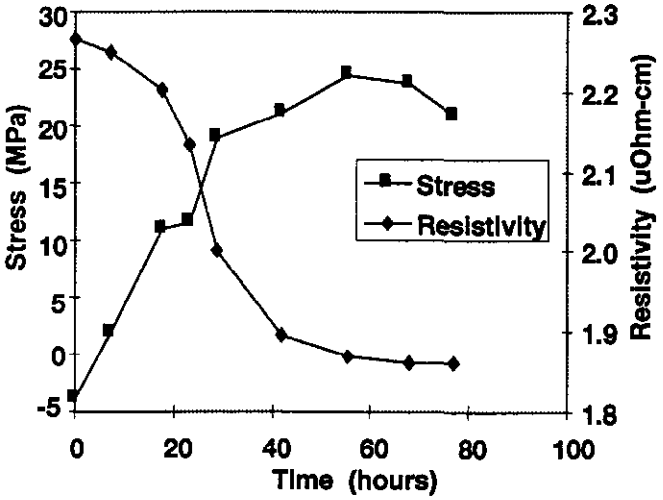


Figure 8- Self annealing effects on stress.

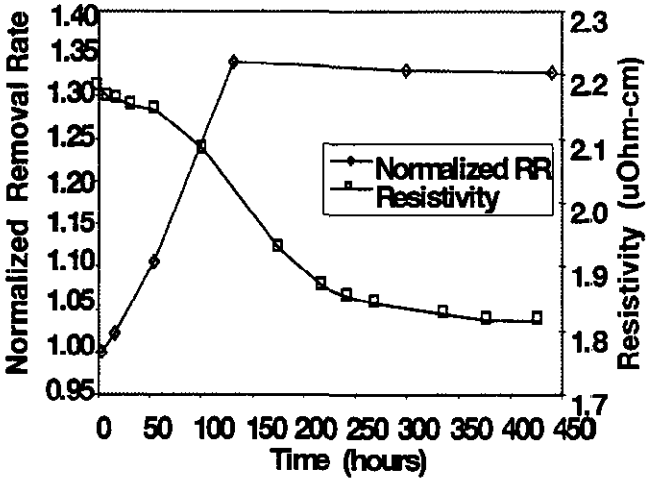


Figure 9- CMP removal rate as a function of self anneal time.

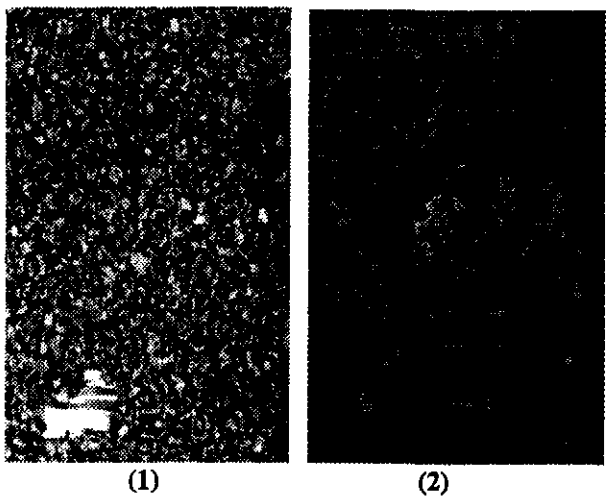


Figure 10 - Grain growth, (1) as deposited grains ~0.1μm (3.9 μ-in), (2) self annealed grains, >1.0 μm (39 μ-in).

Figure 11 - Effect of 120°C anneal on the Cu grain size in 0.25 μm (9.75 μ-in) trenches.

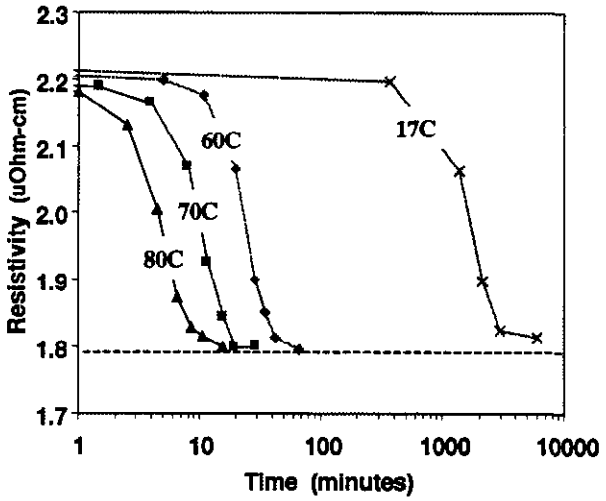
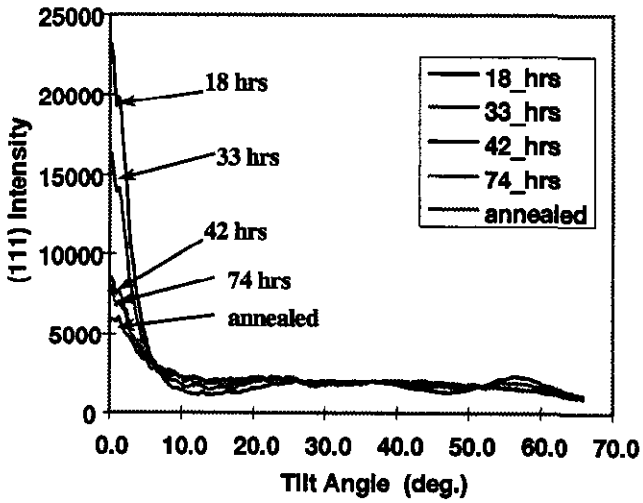


Figure 12- Effects of thermal annealing on the resistivity of the copper film.

Figure 13 shows the effects of self annealing and a post plating thermal anneal on the fiber texture of electroplated copper. Fiber texture plots for the electroplated copper film on blanket wafers showed an initial strong (111) orientation.[13] During the transition period for self annealing it is clear that the (111) texture decreases and the formation of secondary peaks is observed. Texture evolution is specific to the particular barrier material selected and may either strengthen with self annealing or as in this case be reduced as a result of self annealing. The morphological changes observed for thin electroplated copper films suggests the of a thermal anneal process for stabilization.

Figure 13- Effects of self anneal on fiber texture for 1.5μm (58.5 μ-in) electroplated copper film.



Conclusions

Copper electroplating is being implemented into the mainstream fabrication process for semiconductor devices. Copper electrodeposition has been successfully demonstrated as a viable alternative to the traditional aluminum metallization schemes. Semiconductor products will be offered for commercial sale in 1999 that have electroplated copper for interconnects. Control of the electroplating fill mechanism is essential to the formation of defect free copper deposits. Further development and optimization will be required to fully understand the interaction between the copper plating solution, organic additives, and the plating parameters to extend the electroplating capabilities from 0.25μm (9.75 μ-in) down to 0.10 μm (3.9 μ-in) over the next several years. Additionally, control of the electroplated Cu microstructure is key to the manufacturing of reliable integrated circuits.

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