An Overview of Small-Hole Processing

By M.J. Harris

One of the most critical high-density challenges for the 1990s.

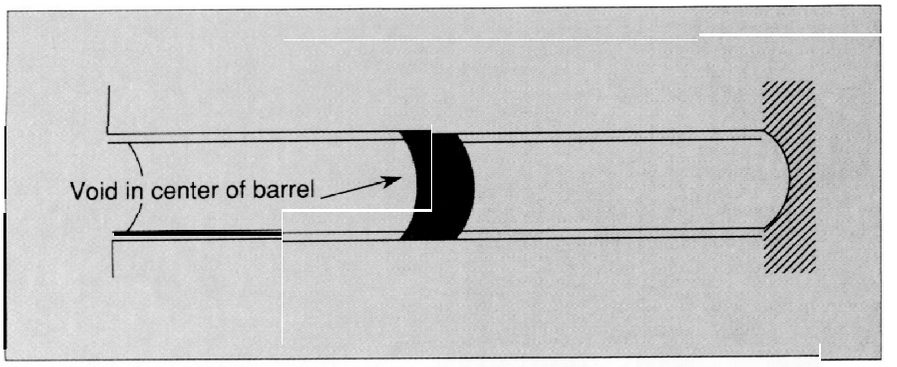

Figure 1A. *Void in high-aspect ratio hole.*

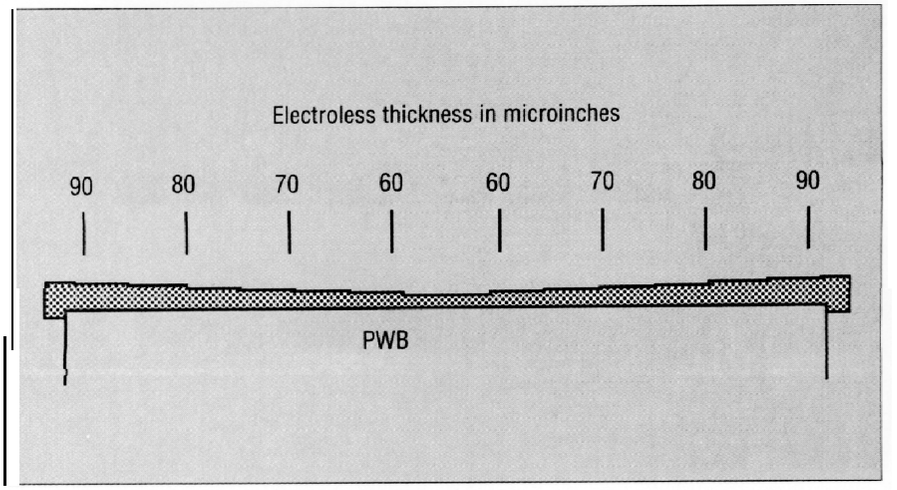

Figure 1B. *Example of poor electroless copper distribution in high aspect ratio hole.*

As SMT becomes more sophisticated, PCB real estate becomes more valuable. Designers will be evaluating the competition for this space. This board area will probably be a matrix of conductors, spaces, on-grid holes for leads and their pads, surface-mount sites, connector tabs, and small holes.

These electrical interconnect holes are high-aspect[1], less than 0.01 2“ in diameter, leadless, non-component-bearing, and frequently off-grid. In addition, they require the same plating specifications as traditional holes. Each panel can contain 5,000 or more holes.

To the designer, small interconnect holes are an elegant solution to the problem of high-density connectivity. This type of hole has been used for years in metallized via technology as well as semiconductor device and chip carrier fabrication. A reduction in layer count often occurs with this creative signal routing; therefore, the use of small holes can be expected to increase.

DEFINITION OF SMALL HOLES

A poll of several fabricators obtained a consensus defining small

Table 1. Initial *review of categories and areas for investigation.*

Lamination	Laminate and prepreg composition, cycles and layer count
Drilling	Drills, drilling techniques, uniformity, and debris removal
Desmear	Chemistry and wetability
Electroless	Conditioning, copper initiation, rates and thickness uniformity, and gas entrapment
Pattern clean	Precleaning, etch-outs, or resist-contamination-preventing plating
Pattern plate	Copper plate distribution and solder distribution
Dynamics	Velocity in barrel (hole wall vs. center barrel vs. center of board vs. hole entrance)
Agitation	One way agitation vs. oscillation, bump, vibration, and solution flow set-up
Racking	Basket (bulk vs. one up), angle, speed, stroke, frequency, spacing, and panel orientation
Processing	Vertical vs. horizontal conveyor (push and pull)
Chemistry	Sequence, constituents, surfactants, rinsing, and diffusion effects

holes to be less than 0.012' in diameter and perhaps as small as 0.006" with continued improvement of drilling techniques. When these holes are combined with board thicknesses of 0.040" to 0.070", aspect ratios of 4:1 to 11:1 result. Boards with 20:1 aspect ratios have been reported.

Unfortunately, the complex boards have small and large holes and cannot be culled for selective processing. This problem is experienced by fabricators attempting to process such boards using traditional and potentially outmoded methods.

Most fabricators begin to experience plating quality variations with holes having a diameter of approximately 0.010" to 0.012".

The most commonly observed defects are circumferential voids and thin plating within the center of the barrel (Figures 1A and 1 B). Occasionally, random plugs or loose debris will generate irregularly shaped defects, but these are more thoroughly understood. With today's required six-sigma confidence levels and the increasing value of each panel, a more comprehensive understanding of the key variables is required.

BRAINSTORMING THE VARIABLES

To address this issue, brainstorming sessions on the subject of the various interactive variables are required. The sessions should involve the participation of key specialists in the areas of process engineering, service, plating, equipment design, chem-

istry, and fluid dynamics. An initial review of the areas of investigation is presented in Table 1.

A complex test vehicle (board) must be carefully designed that encompasses all expected aspect ratios and can generate statistically significant results. A partnership between a well-staffed supplier and a leading-edge fabricator is also required. Evaluation of results must be based on sound observation practices. Comprehensive electrical testing is also important to ensure a positive outcome.

While the theoretical, experimental, and empirical data are being generated, we can practice tips from a broad experience base (Table 2).[2]

Table 2. *Processing tips for small holes.*

Lamination	Adequate press times and temperatures
Drilling	Postbake before and after drilling, follow manufacturers recommended chip loads, complete deburr, and ultrasonic removal
Desmear	State of the art permanganate processing
Electroless	State of the art copper solution with uniform distribution of component replenishment
Pattern clean	Clean developing resist and mild microetch
Pattern plate	Proven uniform high-aspect electrolytic copper and dissimilar metal plating technology
Agitation	4" to 6" full stroke at 16 to 20 strokes per minute with vertical bump at 8 to 10 minutes and cross flow solution agitation (parallel to panels), weir at back of tank
Racking	Basket spacing of ½" to ¾" between panels, restricted from swaying or nesting with 30° vertical angle for gas release
Chemistry	Use proven process sequence designed for best results
Counsel	Use competent supplier with resources to help you

FUTURE TRENDS

Designers will want to continue the trend toward small holes to satisfy packaging needs with the smallest amount of effort. As a result, this trend will persist. Small holes must be viewed as an opportunity to aid the packaging community. ■

REFERENCES

[1]Fisher, G.L., W. Sonnenberg, and R. Bernards. "Electroplating of High Aspect Ratio Holes," *Printed Circuit Fabrication.* 12(4), April 1989.

[2]Prepared from practical and academic information generated in cooperation with Shipley's Corporate Technical Service Department.

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