

Ultrathin Multilayer Circuits

In this alternate configuration, the whole is greater than the sum of its parts.

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The trend toward thinner circuits has revealed a need for improved processing techniques to produce multilayer boards for existing and emerging applications. A new approach to building ultrathin MLBs holds promise for high-density electronic packaging. This article will describe a repeatable, high-volume process for constructing these circuits.

Technology Comparison

A conventional rigid PCB construction incorporating 100-micron core insulators and 18-micron copper for the cap layers results in a finished thickness of 800 microns for a six-layer board.¹ Such a thin copper/prepreg construction creates significant handling challenges for imaging equipment, pushing the technology's capability limits. Conventional flex technology incorporating 25-micron polyimide insulating films, 18-micron copper, and 25-micron adhesive for layer bonding doesn't fare much better, yielding a total thickness of 653 microns for a six-layer design.

The techniques described in this article yield a nominal thickness of 165 microns for a four-layer construction and 355 microns for an eight-layer construction. A combination of vacuum metallization, thin copper metallized through holes, anisotropic adhesives, and thin polyimide coatings is used. Anisotropic adhesive also provides a built-in blind and buried via system, which allows an average increase of 25 to 40% in packaging density. While the product itself is thinner, a reduction in layer count is also often achieved.

Construction Overview

Double-sided circuits are fabricated by vacuum metallization of a thin layer of copper onto both sides of a 50-micron polyimide film.² Via holes are placed in the

base polyimide prior to metallization so that copper can be deposited on the surface and in the via barrel simultaneously. Additional copper is electroplated to a minimum of 5 microns. This technique, commonly referred to as metallized through-hole or MTH, yields the same copper thickness in the hole barrel as on the surface.

In conventional double-sided processing, a clad laminate is fabricated, punched, and plated through to form a configuration in which the barrel copper is thinner than the surface copper.

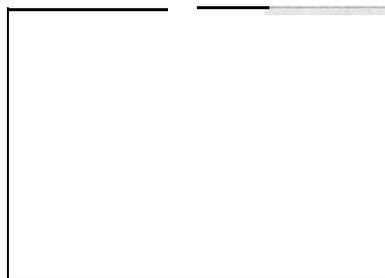


Figure 1a. MTH with 50-micron polyimide and 5-micron copper.

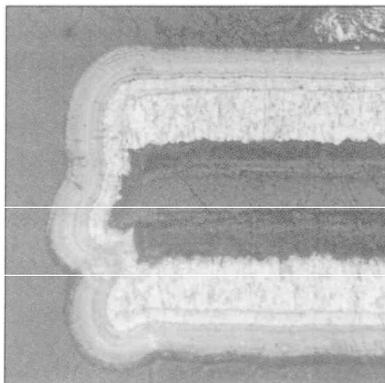


Figure 1b. Conventional flex with PTH construction.

The metallized through-hole technique reduces overall board thickness, and direct metallization without the use of adhesive provides a very robust through hole (Figures 1a and b). The elimination of adhesive on the base substrate substantially reduces Z-axis movement during stress. MTH constructions with only 5 microns of plating on the surface and in the hole barrel have been subjected to 35 kg/cm² at 180°C with no evidence of barrel deformation or cracking. Because the surface copper is the same thickness as that in the barrel, the circuit pattern can be generated by etching only 5 microns of copper. Line resolution is limited only by the etch resist's resolution capability.

After imaging, a thin polyimide coating with access openings for Z-axis interconnection is applied to both the top and bottom copper surfaces. A 5-micron coating thickness was chosen for this construction. The result is a 70-micron-thick double-sided flex circuit with discrete access openings.

Next, the double-sided precursors are connected in the Z axis with a 25-micron layer of anisotropic adhesive.³ Surface treatment of the 5-micron insulator was required to achieve a suitable bond at the interface. After treatment, the layers undergo a final cleaning to remove copper surface oxidation, and a platen pressing step completes the inter metallic interconnections. Table 1 shows the stackup of a completed six-layer multilayer.

Process Characteristics

Layer-to-Layer Insulation

Layers 2/3 and 4/5 are separated by only two 5-micron insulating layers with anisotropic adhesive sandwiched between them. To determine whether or not such a thin covering can provide sufficient insulation resistance and dielectric breakdown voltage, a statistically designed experiment was performed, which examined several factors:

- time delay between surface cleaning and application of the insulator
- orientation of the conductor traces relative to the circuit web
- orientation of the conductor traces relative to the opposing conductor traces
- use of an anti-oxidant after surface cleaning
- insulator formulation.

Table 1. Stackup of a completed six-layer multilayer.

5	Polyimide	
5	Copper	Layer 1
50	Polyimide base	
5	Copper	Layer 2
5	Polyimide	
25	Anisotropic	
5	Polyimide	
5	Copper	Layer 3
50	Polyimide base	
5	Copper	Layer 4
5	Polyimide	
25	Anisotropic	
5	Polyimide	
5	Copper	Layer 5
50	Polyimide base	
5	Copper	Layer 6
5	Polyimide	
260	Total thickness	

* All measurements are in microns.

A 2" X 2" serpentine etch pattern was imaged onto a single-sided 15-micron copper/50-micron adhesiveless base material, and the conductors were insulated with the 5-micron polyimide cover. The coupon was surface treated and then flipped and bonded to an opposing layer of similar configuration using anisotropic adhesive. Although a 15-micron copper thickness was used in the DOE, the same or better results would be expected for 5-micron copper.

A highly significant factor was accidentally discovered during the experiments. A test run was made to evaluate the feasibility of measuring insulation resistance and dielectric breakdown voltage as response variables. The most likely significant factor in this scenario is the time interval between application and drying of the insulating coat. The experiments showed that suitable insulation resistance and dielectric break-

down voltage can be achieved with the new construction.

Current-Carrying Capacity

Designers want to know the minimum size at which they can spec interconnect pads to provide adequate surface area for anisotropic layer connection. Previous studies have shown that a minimum of 1 + mm access diameter must be maintained to obtain a suitable Z-axis connection.⁴ This diameter allows for deformation of opposing layers during bonding. Unfortunately, such large diameters are unsuitable for many high-density applications. But with a dielectric thickness of only 5 microns on each layer, much less compression is required.

A test coupon was constructed from 15-micron copper/50-micron polyimide single-sided material using a daisy chain configuration with sets of 0.125-, 0.250-, and 0.5-mm pads. The daisy chains were linked by 0.125-mm traces.

Table 2. Number of flexes to failure.

# of layers	0-mm radius	1.25-mm radius	2.25-mm radius	7.5-mm radius
4	2	6	6	*
6	1	3	7	*
8	1	1	1	*

*Flexed 100X, no visible effect.

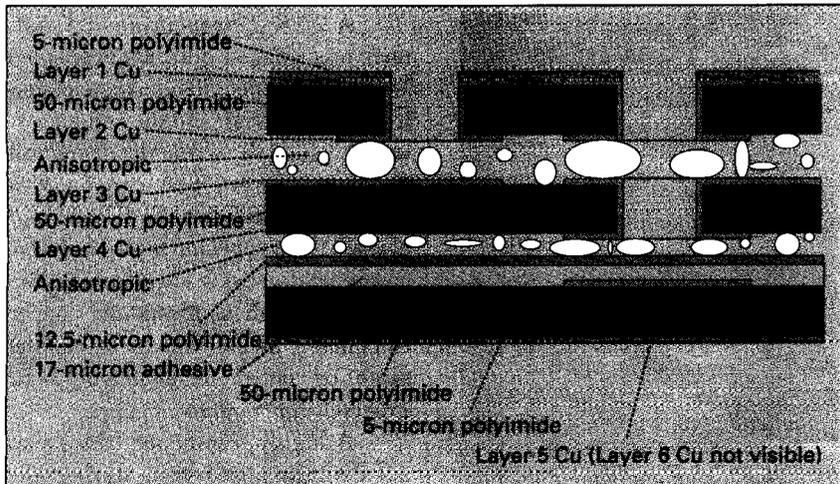


Figure 2. Cross-section of a completed interconnect.

The average maximum current-carrying capacity for all three pad sizes was about 1 amp, indicating that trace width may be the limiting factor. Once the source of resistance variability is controlled, the current-carrying capacity of 0.125-mm pads used for Z-axis connections should be adequate for most high-density applications.

Flexibility

Four-, six-, and eight-layer constructions were fabricated. Based on the neutral axis theory, conductors were located in an I-beam configuration to represent a worst-case scenario for flexing. The results are shown in Table 2.

Much greater flexibility can be obtained by locating traces in the bend area on the central layers, closer to the neutral axis. Flexing studies have been completed on a three-layer stripline controlled-impedance application for a notebook computer. The flex life of the signal layer averaged 50,000+ cycles with a minimum of 25,000. An adhesive-based construction subjected to the same conditions failed between 7,000 and 17,000 cycles.

Sample Application

A six-layer MCM-L was constructed for a personal computer memory card application. Double-sided precursors were assembled with an isotropic adhesive (Figure 2). This application involved inserting a 12.5-micron polyimide with 17.5 microns of adhesive between layers 4 and 5. Layer 4 contained signal traces that required controlled impedance and shielding, so the interconnect was designed in a microstrip configuration in which layers 3 and 5 were used as ground planes.

Microstrip impedance is maximized when the ground planes are equidistant from the center signal layer. To facilitate this, the extra insulating material was sandwiched between layers 4 and 5 to provide approximately the same amount of separation as between layers 3

and 4. Packaging density could be increased by placing additional traces on layer 6.

Future Studies

The Z-axis interconnection has passed MIL-P-50884C qualification testing using adhesive-based double-sided precursors to construct the 10-layer test coupon. Accelerated aging and thermal cycling also attest to the reliability of the Z-axis interconnect in the larger form factor, but additional testing on small-diameter (0.125-mm) pads using the MTH construction is planned.

Insulation resistance and dielectric breakdown voltage must be evaluated under elevated temperature and humidity conditions to ensure that the thin polyimide insulator remains intact.

Conclusion

This new approach to thin multilayer construction yields substantial thickness reduction, enhanced flexibility, and reduced interconnect size and layer count. Additional reliability studies are planned to fully characterize the new technology.

FAB

References

- ¹ Kimura, T., et al. "Commercial Production Technology for Very Thin Multilayer Boards of Five Lines/Pads." Proceedings of Printed Circuit World Convention VI, San Francisco, CA May 1993.
- ² U.S. patent applications #5 112462 and #5 137791 have been filed on this technique.
- ³ Several patent applications have been filed on this technique.
- ⁴ Ibid.
- ⁵ Sweitzer, Brent. "Multilayer Dynamic Flex." Sheldahl Inc., July 1993.

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This paper was originally presented at the IPC's fall meeting, October 24-28, 1993, in Washington, D.C.