

# HIGH-POTENTIAL FAILURE ANALYSIS

by Luis F. Sotto

A study to identify causes of hi-pot failures.

**H**igh-potential (hi-pot) testing verifies nonelectrical continuity between power and ground planes in PWBs. The test is performed by creating a high potential (usually 1,000V) between the different power and ground layers within the circuitry. Voltage is slowly increased at either 50 or 100V per second until it reaches 1,000V. That voltage is then held steady for 10 seconds. If arcing or current leakage above 10 microamps interrupts the potential during the testing period, the circuit has failed.

Hi-pot testing is performed to identify three basic types of defects:

- Resin voids
  - Shorts between power and ground planes
  - Inadequate clearance between power and ground planes.

The following study was conducted to identify most of the causes of circuit board failure and to aid in the understanding, evaluation, and correction of deficiencies in the manufacturing process. Microscopic inspections and evaluations played the most important role in defining defect sources. X-ray fluorescence (XRF) and scanning electron microscopic (SEM) analysis techniques were also used to detect some of the other surface contamination sources.

Because of limitations in the hi-pot test equipment and because pronounced effects are easier to identify, only boards that failed the hi-pot test by arcing (sparks) were used for this failure analysis. A sample group of 709 circuits that failed the test was used for the investigation. The circuits' layer counts varied from four to 10 layers. The defects observed and identified as causes of failure were categorized into two major groups—innerlayer defects and outerlayer defects.

## INNERLAYER DEFECTS

### *Resin Voids*

Resin voids are one type of innerlayer defect. They result from incomplete air withdrawal from boards during lamination cycles in hydraulic, vacuum, or autoclave presses. When air is not properly removed from the lamination books as the resin reaches its minimum viscosity, an air pocket is left. This empty space produces internal electric arcing during hi-pot testing if the resin void is between power and ground planes and is of sufficient size (Figure 1).

The major problem with inspecting circuits for resin voids is that the inspection can only be done when the product is finished. Unless the resin void is left in the outerlayers of the multilayer board, it is almost impossible to visually detect. Further, there is no good repair procedure. These difficulties make hi-pot testing very important.

A variation of resin voids is called resin starvation. This term is normally used to describe a lack of resin in the fiberglass (Figure 2). Resin starvation also increases the propensity for hi-pot failure, especially if the finished circuit has been exposed to high humidity.

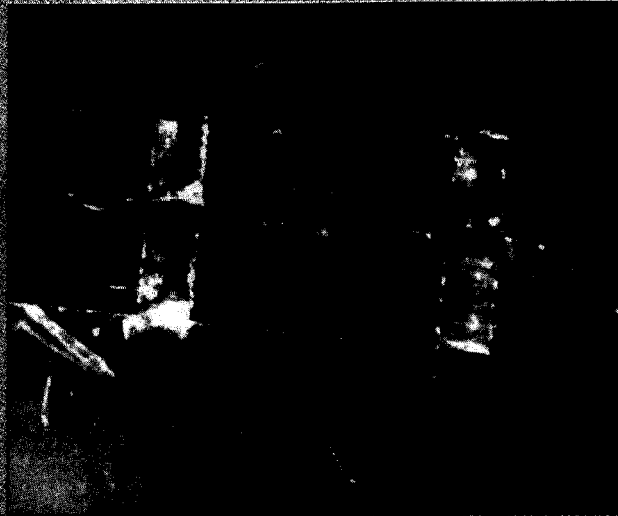
### *Microscopic Delamination*

Delamination may cause hi-pot failure because it produces the empty space between power and ground layers, traces, or holes that causes electric arcing during testing. Delamination is usually not visible to the naked eye nor with magnification of three to seven times during visual inspection.

Figure 3 shows a large delamination area in polyimide material that occurred in the center of the circuitry beneath two big planes. The defect cannot be seen from the outside of the circuit because of the polyimide color.



Figure 3. Bend in innerlayer.



And after solder masking, it is impossible to detect.

The cross-section in Figure 3 also shows a bend in the innerlayers. The change in the circuit thickness is too minute to be read with a caliper or any similar instrument and is very difficult to locate in the board.

#### ***Innerlayer Registration (front to back)***

The front-to-back registration of different innerlayers helps prevent electrical shorts or opens between different networks as well as hi-pot failures. Drill misregistration has the same effect as innerlayer misregistration (also called innerlayer shift). In Figure 4, the innerlayers are not shorted but the clearance to the hole wall is such that arcing occurred.

#### ***Innerlayer Underetch***

In the subtractive fabrication of innerlayers, a copper etching process defines the circuitry. If the foil copper is not completely etched between lines or planes, a microscopic trace of metal will remain. This condition will not necessarily cause a failure during electrical testing (ET), but arcing can occur during hi-pot testing if the metal trace is between the power and ground planes. Depending on the severity of the condition, AOI may or may not detect the defect.

Figure 5 shows incomplete etch. The area in the circuit was easily identified because the arcing caused abnormal delamination.

## **OUTERLAYER DEFECTS**

### ***Surface Contamination***

PCB fabricators are experiencing difficulties with complexity and manufacturing process limitations. Solder mask over bare copper (SMOBC), double-sided surface-mount technology (SMT), and controlled-impedance boards are a few fabrication headaches. Surprisingly,

surface contamination on SMT designs is one of the highest sources of hi-pot failures.

Three basic types of surface contamination that affect hi-pot may occur at any process stage after the copper etching process. More sophisticated inspection equipment—XRF and SEM—was used to identify the sources of these defects; magnification with light microscopes or stereoscopes was not adequate.

***Ionic Contaminant ion.*** Residual ionic contamination can cause surface electrical leakage in addition to chemical and galvanic corrosion. Considering all the chemical processes and solutions used in manufacturing PWBs, a high degree of ionic contamination can be expected if the product is not properly cleaned.

After several tests for ionic contamination at different stages of the manufacturing process, including nickel-gold, fuse, hot-air leveling (HAL), and rout, readings in the range of 0.3 to 0.5 pgr. NaCl per square inch did not represent a problem for hi-pot testing.

***Poor Rinse and Cleaning.*** In this subgroup three chemical processes were considered as possible sources of surface contamination: the nickel-gold, fuse, and HAL processes. Depending on the process sequence and the type of equipment used in different board shops, these three processes may contaminate boards at different degrees.

Most of the problems found during failure analysis for surface contamination were in products coming from HAL. Arcing occurred between surface-mount devices during hi-pot testing because a white residue left by the HAL process was conductive. The SMT footprint shown in Figure 6 is 25-mil pitch. The condition worsens with 12.5-mil-pitch surface-mount footprints. In fact, the latter represents a problem for hi-pot even with a clear space between pads; the clearance is such that arcing takes

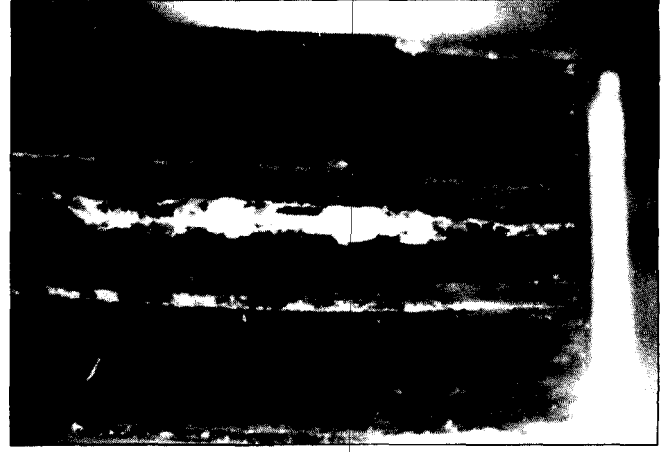
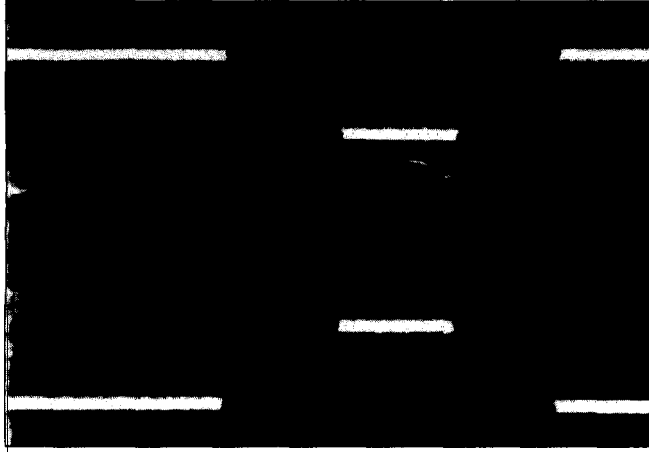


Figure 3. Delamination in a polyimide material.

place. However, circuits having this condition may pass the ionic contamination test. One simple answer exists: the white material was not completely nor easily soluble in an alcohol-water solution, which is the media used for ionic contamination testing.

For preliminary identification of this contamination, an X-ray fluorescent spectrum (XRFS) analysis was done. Figure 7 shows the contaminant, which was found to contain copper, bromine, and tin.

A scanning electron microscope better defines the crystals in the

contaminated surface (Figure 8). Using a collimator aperture of one micron, the SEM's spectrum analysis showed the presence of tin and chlorides. Peaks of gold (Au) and palladium (Pd) are induced into the sample as part of the sample preparation, and a bromine peak matches the fire-retardant component in the dielectric.

After a series of additional tests, it was concluded that the stannous chloride was coming from the combination of the hydrochloric acid in the flux and the solder in the pot. Because of a poor flux rinsing after solder

coating, flux residues were trapping the stannous chloride. Once the circuit is dried, removing the flux using only water is very difficult. The chloride contamination can't be removed with high pressure water or pressurized air. strong organic solvent such as 1 1 1 -Trichlorethylene is needed.

This electrically conductive contaminate as not necessarily bridging the surface-mount pads but was substantially reducing the spacing. Consequently the circuits failed hi-pot because of arcing.

Effects of Router Dust. Circuits



Figure 4. Poor innerlayer clearance to the hole wall causes arcing.

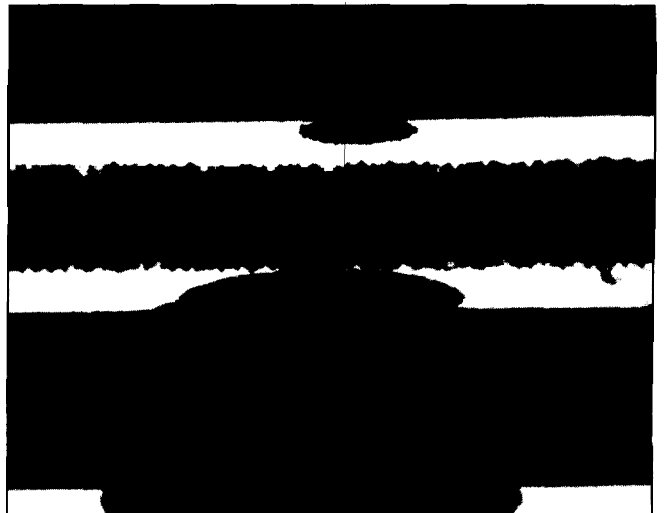


Figure 5. Incomplete etch.

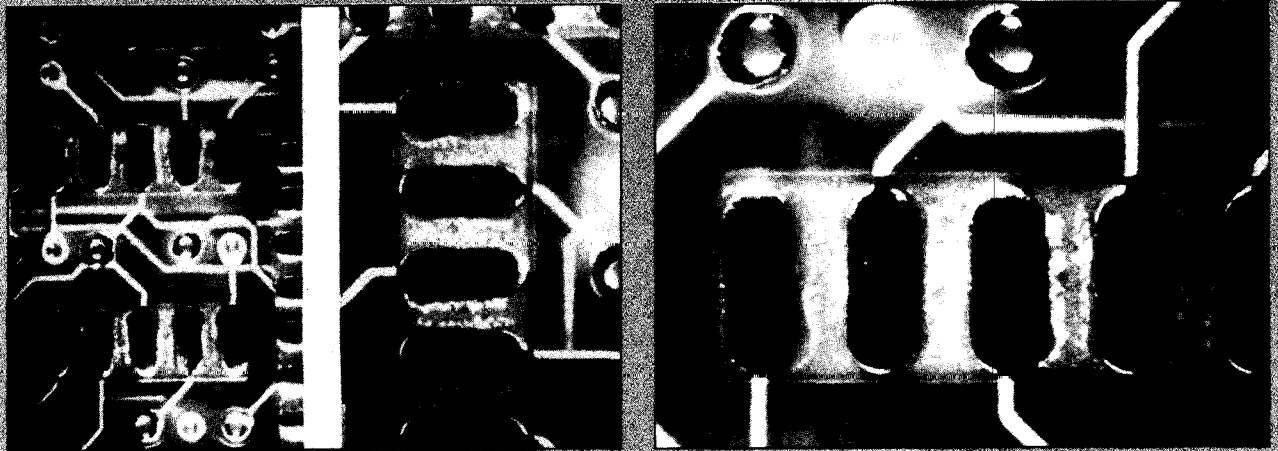


Figure 8. Contaminated surfaces with white residue after HAL.

arcing between surface-mount devices exhibited an interesting condition—the presence of very fine, clear crystals (Figure 9). SEM analysis results showed silica (Si) and chlorides (Cl). These elements are the basic components of the fiberglass. More extensive XRF and SEM analysis indicated that the material observed was coming from the board itself during muting. The hypothesis was confirmed by contaminating a group of circuits with router dust coming from a clad panel (just the dielectric).

A theory was developed based on the behavior of the contaminated circuits' testing patterns. The potential was increasing to 1,000V but then wouldn't hold that voltage. A few seconds after reaching 1,000V, arcing occurred, and the test subsequently failed. It seemed that the material was ionized as the high potential was being held. This theory was difficult to prove, but it was observed that router dust reacted to a magnetic field. To decontaminate the circuits with this condition, high-pressure air was used to blow the dust off the surface-mount devices.

#### ***Underetch and Overetch***

***Incomplete copper etch.*** The defects that will affect the quality of boards built in the future are not all different from the problems of today and yesterday. The basic difference is that today's defects are not as easily detected by the inspection systems found in most PCB fabrication shops. Also, with more sophisticated PCB designs and requirements, what was neglected in the past is now a problem.

Figure 10 shows an incompletely etched circuit. No electrical connection exists between surface-mount pads but the clearance allows arcing to occur during hi-pot testing, making the circuits fail immediately. The underetch condition is difficult to see with magnification of seven times. Figure 11 shows surface-mount devices with 25-mil pitch. The dielectric surface between devices shows that a microscopic track of metal was left between surface-mount pads. It stops as it nears the center. This circuit was arcing between the two pads.

***Overetch.*** Copper overetching creates either copper or tin-lead slivers that are in some cases as small as a hair. If the slivers bridge power and

ground, the circuit will fail hi-pot immediately, otherwise arcing will occur. This problem can be identified by tape testing the failing circuits and looking for any slivers.

#### ***Partial Solder Webbing***

Partial solder webbing is caused by the hot-air solder level process. If excess solder is not removed correctly from the circuit, it leaves a virtual solder connection between the lines, holes, and surface-mount pads. Because of the critical clearance between the surface-mount pads, they are more prone to this type of defect (Figure 12). Partial solder webbing does not always cause a failure. If the two pads are not connected to power or ground, the circuit will pass electrical and hi-pot testing. However, this condition may cause electrical shorts during board assembly as a consequence of the solder paste screening.

#### ***Electrical Test and Repairs***

Circuits with repaired shorts will fail hi-pot because the repair at electrical test was good enough to break the shorts but not good enough to prevent electrical arcing. Figure 13 shows repaired shorts between the surface-mount pads. The metal left

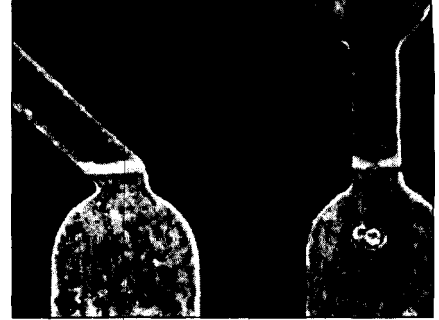
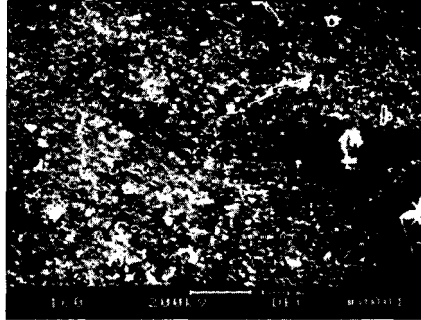
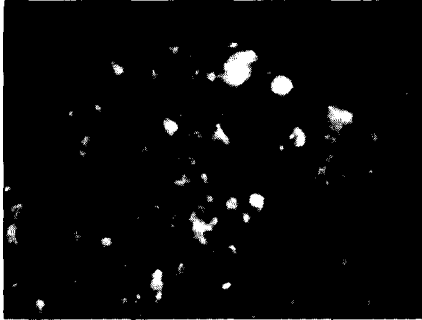


Figure 8. SEM of crystals on contaminated surface.

between these pads reduces the overall spacing.

The preparation of test fixtures to electrically test the different networks in circuit boards could be a problem. Since test point sizes are becoming smaller (for example, SMT devices), the quality of the pin in terms of deflection (side movement) must be considered more carefully. Also pin registration when preparing test heads is more critical. Test pins resting right in the edges of small surface-mount devices have a tendency to chip off metal particles (solder). These particles reduce the spacing between pads making arcing possible during hi-pot testing.

## CONCLUSIONS

Printed circuits with relatively high aspect ratios, high innerlayer counts,

and very small surface-mount devices are more likely to fail. Their failure cannot be attributed to one specific cause, however. The cause may vary from week to week and month to month. Quantifying different defects is difficult because the defects can't be precisely identified in every circuit failing the test.

At the beginning of the investigation, the failure was thought to be laminate voids. As more and more circuits were analyzed, a whole range of different defects was found, including defects so microscopic that their existence was never precisely detected. In other hi-pot tests, the defects causing the failures simply could not be found.

Almost all the defects described in this article can only be found using higher magnification than normally

used to inspect product. As circuit technology gets more complex, defects are no longer very visible. Visual inspection tools must be upgraded. Problems with manufacturing processes cannot be corrected unless defects are seen.

There is no universal cure for all the circuits failing hi-pot testing. Every processed circuit or batch must be analyzed individually to find the cause of failure. The behavior of the voltage during testing as well as the magnified inspection of the failures play a very important role in the troubleshooting technique used in circuit testing. ■

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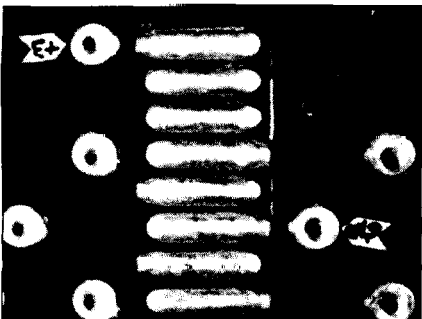


Figure 10. This circuit is incompletely etched.



Figure 11. Microscopic metal track between SMT pads.

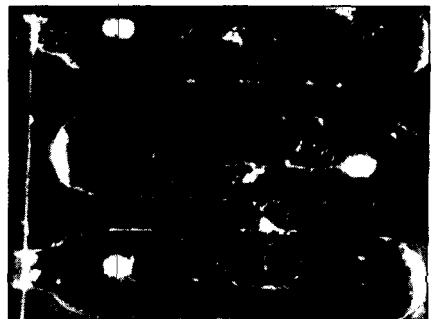


Figure 12. Solder webbing between SMT pads.