Evaluating Etcher Performance

Fine lines call for different standards.

Don Ball

I am often asked what level of performance can be expected from etching equipment when processing fine lines. These tolerances are usually expressed as a range in percentage form (e. g., ± 5% on 4-mil lines).

Since the question of performance level is typically posed by people who have little or no experience with high-density, fine-line etching, a basic outline of how to analyze etcher performance proves helpful.

The Building Blocks of Performance

Each step in the PCB manufacturing process contributes to overall line width variation, and each contribution is cumulative. As lines and spaces shrink, the impact of each individual factor grows.

Up to a point, the role of most process steps that precede etching is relatively minor, and the etcher is usually the first thing to be checked when line widths fall out of spec. After all, this is the point at which line widths are generally checked for the first time. Thus, the industry has come to equate line width variation with etcher performance.

When lines and spaces fall below 5 roils, the processes prior to etching assume an even greater role. A ± 5% line width specification for a 10-mil line yields a line width window of 9.5 to 10.5 roils. The same spec for a 3-mil line yields a window of only 2.85 to 3.15 roils. Most shops can hold a ± 0.5-mil tolerance on a 10-mil line without much difficulty, but a ± 0.15-mil tolerance on a 3-mil line is a different story.

The following example will help clarify this point. Recently a test was run to track the variation in line widths on a series of panels as the product progressed through the steps required to generate a fully etched panel. The 18" X 24" panels had a test pattern comprising 4-mil lines and 5-mil spaces. The phototool was made via a direct laser plotter, and a new exposure unit with a highly collimated light source was used.

It was found that the line width variation on the phototool was + 2.2%, after developing it was ± 8.3%, and after etching it was ± 10.2%. The contribution of the etcher to overall line width variation was ± 1.9%, while the process steps prior to etching contributed ± 8.3%. If these test panels had been actual product required to meet a ± 5% final line width spec, then the process steps prior to etching would have to be evaluated for opportunities to reduce the variance. The etcher cannot be expected to "improve" the panel it's given to process.

Contributing Factors

Next, we'll evaluate the contributions of the process steps to overall variation, and what can be done to control these influences.

Copper Foil

Copper foil varies in thickness, typically at a level of ± 10% for 1-oz. foil. The ratio between the width of the space and the total height of the sidewalls (foil thickness + resist thickness) becomes very important when etching spaces under 5 mils. The higher the sidewall, the lower the etch rate at the bottom of that sidewall, due to the fact that it is more difficult for fresh etchant to penetrate to the etchant/copper interface. Thus, areas with thinner foil will etch at a slightly faster rate than those with thicker foil.

Phototools

Most phototools are currently made using a digitized image in combination with a computer-controlled laser plotter that directly prints the image on the film. However, this process allows variation to creep into the line widths. Many

companies now use these first-generation tools to directly print their critical-tolerance panels, but many others still use them as masters to make copies to be used for imaging the panel. The process of copying introduces more variation in the line widths.

Phototool type also has an effect on variance due to differences in the refractive indexes of various phototool materials and response to changing environmental conditions in the printing room.

Circuit Design

One influence on the variability of overall line widths that is often overlooked is circuit design. Lines that are configured at right angles with one another are etched at slightly different rates depending on the hydraulic design of the etcher. This phenomenon, due to flow effects at the copper surface, becomes significant when processing sub-5-mil lines and spaces, which are more subject to boundary layer effects.

Circuit density also has a critical impact on the variation in etched line width. An isolated line is etched faster than a line running closely parallel to other traces. As the spaces between lines shrink, this difference in etch rate grows, for reasons explained in the preceding discussion on sidewall height. This discrepancy can range from 0.5 to 1 mil depending on the density and isolation of the respective lines.

Prelamination Cleaning

Whether mechanical scrubbing, pumice scrubbing, or chemical cleaning is used, the purposes of this operation are to remove the top layer of copper and any surface contaminants, and to provide "tooth" to facilitate resist adhesion.

The degree of evenness with which the copper is removed from the panel surface determines the degree of variation introduced during this process step.

There is no way to obtain an accurate estimate of how much variance is introduced at this stage, but because the quantity of copper removed is small, cleaning is probably just a minor contributor. Still, an unevenly worn brush, embedded pumice particles, or a clogged nozzle can still make a significant difference in foil thickness.

Etch Resist

Etch resists-both dry film and metallic—vary in thickness. This fluctuation, in turn, contributes to etch rate variation caused by sidewall height variation.

UV Exposure

Any variation in lamp output will affect line width since different

exposures impact the width of developed dry film. Lamp temperature, variations in line voltage, and the age of the lamp itself cause substantial discrepancies in lamp output.

Vibrations transmitted to the exposure unit from its environment, e.g., those generated by air conditioning units and traffic, can also have an effect on exposure. In addition, vacuum drawdown time has a significant impact; the closer the contact between the film emulsion and the etch resist, the smaller the variation in line width.

Developing

The developing process is subject to the same problems as the etching process: clogged nozzles, uneven spray pressures, and bath control. There is a little more room for error here since the sidewalls of the resist are well-defined (providing the preceding processes were performed correctly) and not as subject to undercut as is copper in the etching process. Yet, it is still possible to under- or overdevelop a panel, thereby introducing additional variation.

Conclusion

In attempting to determine etcher performance, it's important to keep in mind that what may be considered a broad specification for most products (i.e., ± 10%) is a tight specification when processing features under 5 roils. As a result, different standards must be used in evaluating etching performance in a fine-line scenario. The pointers in this article should help to minimize line width variation in today's higher-density PCBs. FAB

Don *Ball is a senior process engineer with Atotech USA, State College, PA.*