Circuit Technology

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Design for Manufacturability

To remain competitive, PCB designers are prescribing lighter/smaller/denser interconnects in order to accommodate faster processing speeds and greater signal integrity with high-speed computing and signal processing. These mandates impose a significant cost escalation in the cost of printed wiring boards. Thorough scrutiny of advanced material and a more precise manufacturing process to attain denser interconnects is critical. Layout, fabrication and assembly planning is called "design for manufacturing" (DFM), or predictive engineering. Understanding the complexity of fabricating/testing and assembling/testing PCBs is essential for cost-competitive manufacturing. An extensive study by General Electric Co. concluded that 75 percent of recurring manufacturing costs are determined by design drawings and specifications.[1]

Design for manufacturability must carefully scrutinize the need for all items on previous drawings and specifications, with relation to developments in materials, manufacturing techniques and equipment. A team approach is indicative.

High-density Challenges

PCB assemblers are using advanced bonding techniques to improve efficiency and reliability for components with >200 I/Os. These include wire bonding, tape automated bonding (TAB), ball grid array (BGA), flip chip, micro ball grid array (MBGA), tape ball grid array (TBGA) and direct chip attachment (DCA).

To keep pace, PWB fabricators must provide surface finishes that are solderable (with "no-clean" fluxes) and wire-bondable, with planarity required for placement of ultra-fine-pitch components. They also must refine techniques to efficiently process <0.127 mm (5 mil) lines and spaces, thinner multilayers, narrower vias, blind vias and buried vias. Higher-density circuitry and processing speeds will also impose improvements in the properties of dielectric material.

PWB Manufacturing Complexity

Electrical engineers must consider associated costs of fabrication and assembly when introducing new designs that will maximize advances in semiconductor technology. An example of a synergistic approach can be found in a news item in *The Wall Street Journal*, July 14, which states that one computer company has transformed its low-priced computer into one of the more profitable products. Traditionally, low-priced computers have been associated with low profit margins.

A team approach—designers, assembly, fabrication and component engineers—was crucial for design of an interconnect system that was compatible with readily available inexpensive components, with proclivity to maximize the efficiency of high-volume production. This interconnect system scrupulously examined a fabrication complexity matrix to determine absolute essentials for maximizing advances in integrated circuit technology, while utilizing existing assembly equipment to full potential. Material and procedure additives to the complexity of manufacturing printed wiring boards are shown in the matrix.

Fabrication Complexity Matrix[2]

	Highest	High Middle	Low Middle	Lowest
Material of construction	PIM	CE	FR-4	CEM III
No. layers	>8	6	4	DS
No. holes/panel	>20,000	<20,000	<10,000	<3,000
Min. lines/spaces	4 mil	5 mil	6 mil	8 mil+
Gold tabs	3 sides	2 sides	1 side	none
Annular ring	2 mil	4 mil	6 mil	8 mil+
Solder mask	2 S DF	2 S LPI	1 S LPI	UV TC
Surface finish	SSD	Ni/Au	HASL	OSP
Min. via	<8 mil	9-12 mil	13-20 mil	>20 mil
C imp. tolerance	±5%	±10%	±20%	None

Currently, the majority of PCB assembly is performed by contract manufacturers (many also provide design service or work closely with OEM designers) to ensure manufacturability. There are few contract manufacturers that fabricate PWBs and also assemble PCBs. PWB manufacturing is a separate industry.

An understanding of both fabrication and assembly capabilities is crucial in selecting the optimal design, construction, materials, surface finish and components for a particular application. A synergistic approach is essential to provide a design that satisfies reliability, manufacturability, performance and cost issues. **P&SF**

[1] *General Electric, "Review of DFM Principles," Internal DFM Conf., Charlottesville, VA (1982).*
[2] *Clyde F. Coombs,* Printed Circuit Handbook, *4th ed., Ch. 7.18, McGraw-Hill, Inc. (1996).*