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Flip-chip Technology on PWBs

One form of this technology, known as controlled collapse chip connection (C4), was first introduced by IBM in 1964 for use in hybrid circuits. Since that time, other techniques for flip-chip attachment have been developed to attach components to interconnect substrates. Flip-chip processes now in use are gold, solder or epoxy-based technologies.*

These processes are finding applications in telecommunications, consumer electronics, LCDs, watches, PCMCIAs, military electronics and optoelectronics. Until recently, these applications have been on ceramic substrates, because of the thermal coefficient of expansion (TCE) mismatch between silicon and a laminate substrate. By employing an epoxy underfill technique, it is now possible to directly attach silicon chips to laminate substrates. This procedure effectively negates the thermal mismatch problem by distributing stresses over the entire area of the chip.

Flip-chip Attachment Of Bare Die on PWBs

The most economical procedure for producing solder deposits on PWBs is screening and reflow of solder paste. This approach appears to be limited to contact pad pitches >200 microns (0.0079 in.). For finer pitch, microelectroplating techniques are required.

Flip-chip die attach processes have been developed to support pad-limited IC designs, allowing semiconductor designers to take advantage of this packaging technology to place pad sites in an array on the surface of the die, rather than just around the perimeter.

To define flip-chip technology, the following characteristics must apply:

- Face-down mounting of bare die directly on a substrate

- Bumps on one of either the component or substrate
- Substrate footprints mirror image to chip contact pads
- Electrical and mechanical attachment attained simultaneously

Electroplating Role

Tin/lead alloys are plated on bonding pads of ICs, which are turned upside down and are attached to a matching pattern on the substrate. For low-temperature applications, the eutectic Sn/Pb 63/37 alloy (melting point 183 °C or 361 °F) is preferred, while high-temperature requirements favor the lead-rich alloy 5/95 (melting range 270–312 °C or 518–594 °F).

This technique utilizes a photoresist to expose the bonding pads. The cavity created by the resist is filled by a Sn/Pb electrodeposit of the desired alloy. Deposition time to create a solder bump of 45 µm at a current density of 1.4 A/dm^2 is approximately 180 min. The resist is then removed and the solder alloy is reflowed, creating the bump.

Depositing a tin/lead alloy only into the vertical walls of resist windows requires a precisely controlled and maintained process to guarantee:

- A high-purity deposit
- Compatibility with photoresist
- Excellent throwing power
- A constant deposition rate

A methane sulfonic acid-based electrolyte is preferred and frequent replenishment of bath chemicals is essential. Particularly crucial is the selection of grain refiner and oxidation inhibitor additives, which can easily be monitored and are effective in low concentrations.

Successful solder bumping by electroplating techniques requires precise manufacturing procedures:

- Control of all chemicals in the electrolyte within narrow limits
- Purification with activated carbon to limit buildup of organic breakdown products of additives
- High-purity anodes (electrolytically refined Sn/Pb)
- Accurate calculation of plating area
- Pad design to facilitate uniform current density
- Technical support capable of rapid analysis and precise replenishment of chemicals

The eutectic alloy 63/37 Sn/Pb has a melting point of 183 °C (361 °F), and is ideal for bonding with a minimum of heat input. The high-lead alloy 5/95, with a melting range of 270–312 °C (518–594 °F), has adequate wetting characteristics and provides standoff when combined with 63/37 Sn/Pb, where the bumps do not collapse during flip chip attachment.

For applications requiring contact pad pitches < 200 microns (0.0079 in.), flip-chip technology relies on electroplating for accurate attachment of IC to PWBs. By depositing both low- and high-melting alloys, a gap between the IC and PWB can be maintained, if the reflow process is controlled so that the bumps do not collapse during flip-chip attachment.

By filling this space with epoxy, stresses are distributed over the entire area of the chip, minimizing the thermal mismatch problem of silicon and organic substrates. This technique now permits reliable flip-chip attachment to PWBs. **P&SF**

** A. Gemmler, W. Leonhard, H. Richter & K. Ruess,* Proc., Session F, *AESF SUR/FIN®, Cleveland, OH (June 1996).*