Electrodeposition Behaviors of Solder Bumps from Fluoroborate & Sulfonate Baths

By K-L. Lin & K-T. Hsu

Flip chip solder bumps have been electrodeposited from fluoroborate and sulfonate baths to compare the performance of these two baths with respect to growth behavior, composition and bump height of the eutectic solder bumps on a 4-in. silicon wafer. In general, the fluoroborate bath gives rise to a slower deposition rate than the sulfonate bath, while a slightly better bump uniformity is achieved. The solder bumps exhibit a smooth surface appearance when electrodeposited from a sulfonate bath.

Electronic packaging technology has moved from through-hole technology to surface mount technology since the mid-1980s.[1] Recent developments further apply area array I/O arrangements, replacing peripheral arrangements. The area array arrangement makes use of the whole area of a die or substrate compared to the peripheral area arrangement. Accordingly, a greater I/O number can be produced on a die for a fixed pitch size. On the other hand, the pitch size can be enlarged when the I/O number is fixed. A greater I/O number enables integration of more functions within a chip, while a large pitch size lowers inductance, thus enhancing clock speed. Currently, the Ball Grid Array (BGA) represents area array technology. The I/O can very easily go up to more than 500 with BGA in comparison to 300 or so with QFP (Quad Flat Packaging). BGA is a module level packaging technology, while the chip level packaging of a BGA module can incorporate wire bonding, TAB (Tape Automated Bonding), or flip chip bonding technology.[2] To comply with the high I/O area array technology of BGA, it is desirable to apply flip chip bonding for chip level interconnection. Flip chip bonding technology is also an area array technology and is by far the highest I/O chip level packaging technology.

Flip chip bonding technology relies on solder bumps, produced on silicon chips, for interconnection. The solder bump can be produced on the terminal pads by vapor deposition,[3] screen printing,[4] as well as electroplating.[5] Electroplating technology allows the manufacturing of fine-pitch, small-volume solder bumps when incorporated with photolithography. A complete solder bump structure consists of UBM (Under Bump Metallurgy) layers and the solder plating. A variety of UBM layers has been developed.[4-10] The function of a UBM layer is to promote the adhesion, wetting, and to provide a barrier function for inhibiting interdiffusion between solder and the conductor, for example, an aluminum pad. Solder plating needs to be well controlled to produce uniform solder bumps. Electroplating bath conditions and electrochemical cell design may determine the plating behavior of solder bumps. The I/O pad acts as the electrode for electroplating. A chip may contain hundreds of bump pads. Because a wafer contains hundreds of chips, it may be assumed that thousands of solder bumps will be plated simultaneously during the plating process. The uniformity of the solder bump height can be controlled with appropriate cell design.[11] In addition, bath type may also be of importance in controlling bump height uniformity. This investigation discusses the plating behavior of solder bumps with two different baths. The bump height, bump composition and the operating conditions are also investigated.

Experimental Procedure

The procedure for producing the solder bumps on a 4-in. silicon wafer is as follows. An aluminum film with a thickness of 1.5 μm was produced by sputtering on the silicon wafer. The Al film was then spin-coated with photoresist and the wafer exposed under UV light to develop the patterns for solder bumps with the aid of a mask (Fig. 1). The assignment of the chip position is also specified in Fig. 1. Each chip contains 32 x 32 bumps of which the diameter is 60 μm individually. The pitch size, center-to-center distance between neighboring bumps, is 140 μm.

The UBM of the solder bump consists of, sequentially, sputter-deposited 0.4 μm Ti and 0.8 μm Cu, and an electroless nickel deposit. The UBM layers were produced on Al film. The electroless nickel deposition was conducted in a nickel sulfate bath, using sodium hypophosphite as reducing agent.[11] The thickness of the EN layer is around 4 μm. Solder was electroplated from a fluoroborate bath,[11] or from a commercial sulfonate bath. The solution was stirred with a magnetic stirrer during plating operations. The anode was a platinized titanium mesh. The morphologies, as well as the compositions of the platings were investigated with a scanning electron microscope equipped with EDS (Energy Dispersive Spectrometer). The bumps investigated were the center bumps of the arrays located at the diagonal of the upper left quadrant on the silicon wafer.

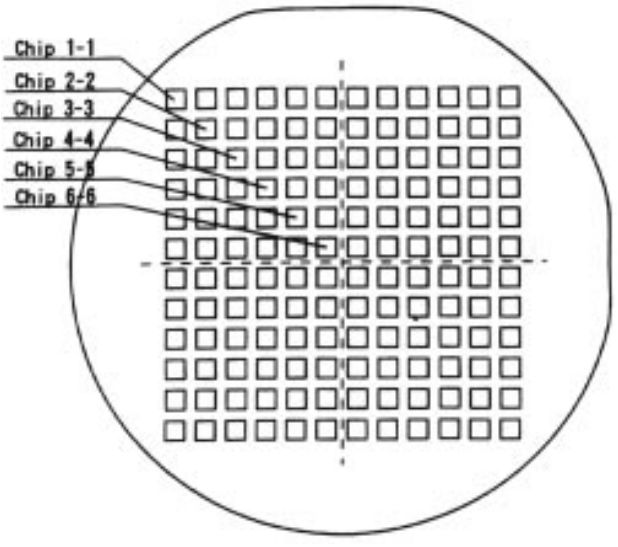

Fig. 1—Chip pattern across a 4-in. silicon wafer.

Results and Discussion

Bath type may significantly affect the current distribution and current efficiency. This investigation was not to analyze current efficiency; rather, it was to investigate the effect of bath type on solder bump growth, as well as on solder bump composition. Figures 2 and 3 depict the solder bumps obtained from a fluoroborate bath and a sulfonate bath, respectively. This series of experiments was performed on Cu plates. The current density ranges are 10-20 mA/cm^2 and 10-100 mA/cm^2, respectively, for fluoroborate and sulfonate baths. It is evident that the bump surface consists of smaller bumps when deposited at 15 and 20 mA/cm^2 from the fluoroborate bath. This mini-bump structure indicates inadequate control of the bump height at these current densities. On the other hand, the bump morphology is relatively smooth when deposited at a current density as high as 100 mA/cm^2 from the sulfonate bath (Fig. 3). The evidence of Figs. 2 and 3 indicate that the fluoroborate bath is not practically appropriate for high-current-density solder bump deposition.

The uniformity of the bump height and the thickness of the plated solder bump are of importance in terms of flip chip bonding practice. This study investigated the average bump height distribution throughout a 4-in. silicon wafer for the sulfonate bath to determine the most suitable current density. The total charge applied was fixed at 108 coulombs. It is seen from Fig. 4 that the average bump height on each chip varies

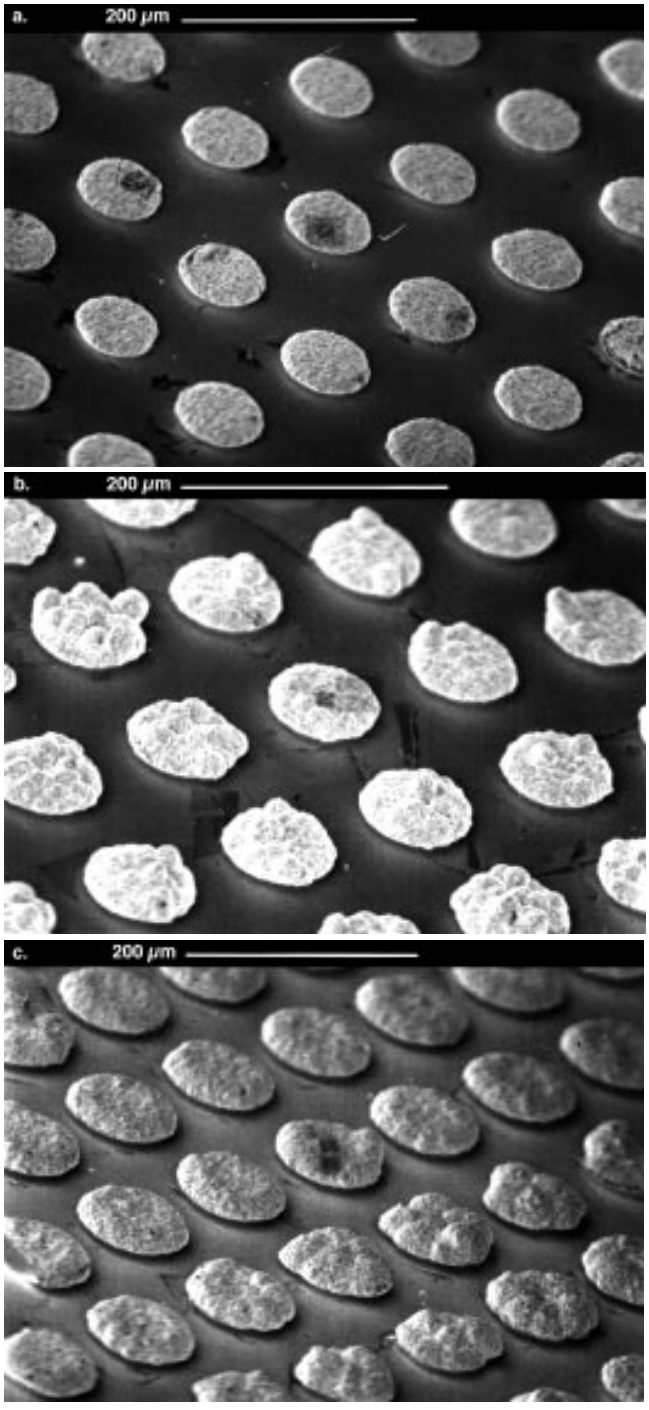

Fig. 2—Appearance of solder bumps electrodeposited from fluoroborate bath, current density (mA/cm^2): (a) 10, (b) 15, (c) 20.

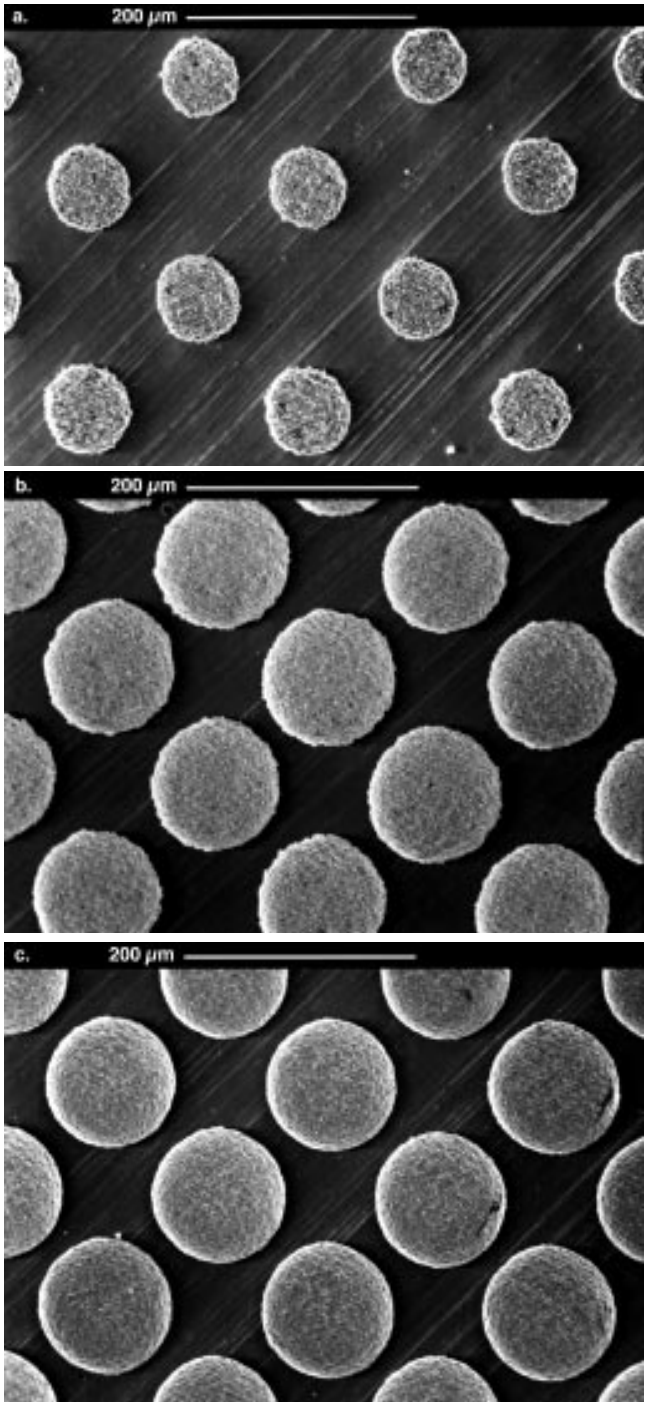

Fig. 3—Appearance of solder bumps electrodeposited from sulfonate bath, current density (mA/cm^2): (a) 10, (b) 30, (c) 100.

from about 20 to 30 μm when deposited at 10 mA/cm^2. An increase in current density to 30 mA/cm^2 not only increases the bump height, in the range of 37 to 40 μm, but also enhances the bump height uniformity with a deviation of 3.3 percent. A further increase in current density raises the deviation to 5.1 percent when the current density is as high as 100 mA/cm^2, although the bump height increases up to 40 to 45 μm.

The solder bump must reflow at suitable temperature to produce a ball-shaped bump for flip chip bonding application. The reflow temperature is determined by the composition of the as-plated solder bump. It is desired to produce the eutectic solder bump, 63Sn-37Pb, to give the lowest reflow temperature. Figure 5 shows the composition of the bumps at different chip positions when plated at various current densities from the sulfonate bath. The total applied charge is 108 coulombs. The Sn content of the bumps varies from 60 to 68 percent Sn (analyzed with EDS) when the current density is 10 mA/cm^2, indicating unsatisfactory uniformity in deposition potential across the wafer. The percent Sn tends to increase as the current density increases from 30 to 100 mA/cm^2. Of these various conditions, a current density of 30 mA/cm^2 results in a composition between 60 and 63 percent Sn and the least deviation in composition distribution.

It is shown in Fig. 4 that current density affects the bump height distribution. In addition to current density, the chip position on the wafer may also affect bump height. The effect of chip position on bump height is ascribed to current distribution. Figures 6 and 7 show the average bump height of each chip across the wafer when deposited from a fluoroborate bath and a sulfonate bath, respectively, with current densities of 10 and 30 mA/cm^2. It is reasonable to achieve a slower deposition rate from the fluoroborate bath. On the other hand, deviation in bump height is seen for both systems, but, for the same bump height range of 30 to 35 μm and 35 to 40 μm, it seems that the fluoroborate bath results in better uniformity. The bump height deviation from the average bump height is 1.08 percent (for 30 to 35 μm) and 2.08 percent (for 35 to 40 μm) for bumps deposited from the fluoroborate bath, while it is 3.02 percent and 3.30 percent from the sulfonate bath. The deviations are all within 5 percent and may be acceptable from the application point of view.

Findings

The electrodeposition behavior of solder bumps has been compared for fluoroborate and sulfonate baths. The deposition rate is much faster from a sulfonate bath than from a fluoroborate bath. A smooth surface morphology of the solder bump is obtained from a sulfonate bath, while a rough appearance is achieved from a fluoroborate bath. A current density of 30 mA/cm^2 results in best uniformity in composition and bump height of the eutectic solder bump deposited from the sulfonate bath across a 4-in. silicon wafer. The fluoroborate bath gives rise to slightly better uniformity in bump height than the sulfonate bath, but both baths give rise to practically acceptable bump height uniformity for their deposition conditions.

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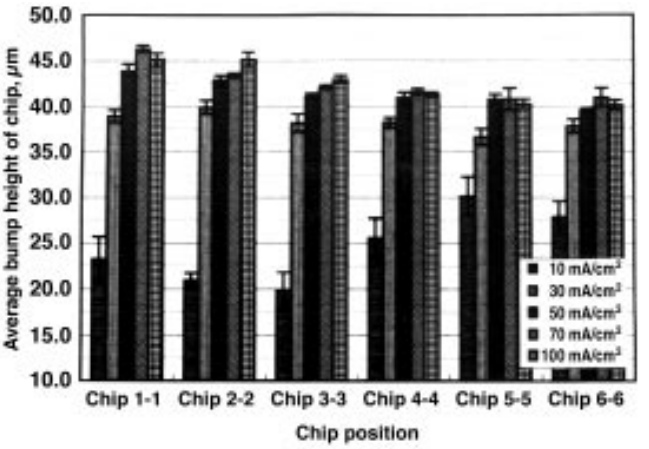

Fig. 4—Average bump heights on various chip positions when deposited from sulfonate bath at different current densities.

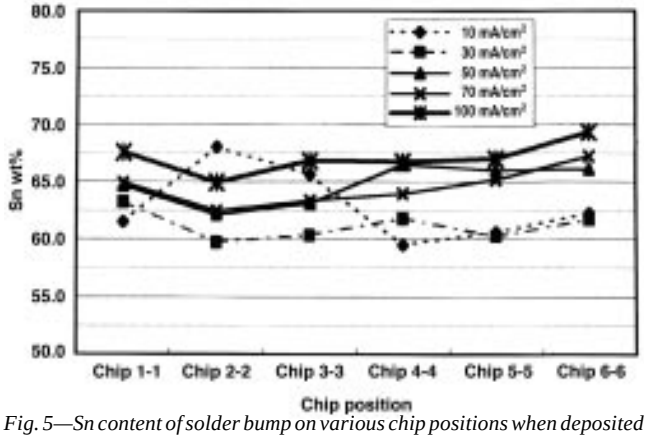

Fig. 5—Sn content of solder bump on various chip positions when deposited from sulfonate bath at different current densities.

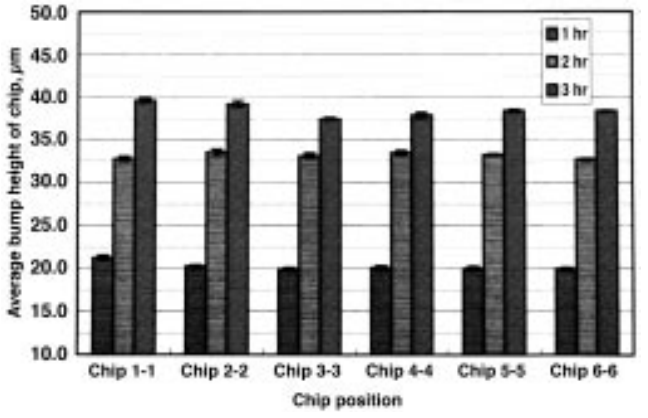

Fig. 6—Average bump heights on various chip positions when deposited from fluoroborate bath at 10 mA/cm^2 for different electrodeposition times.

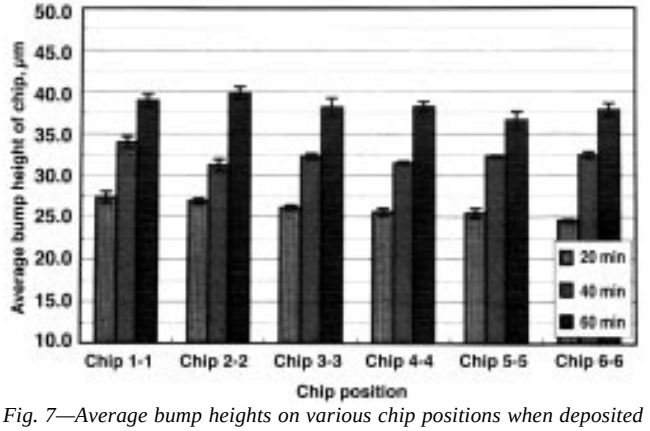

Fig. 7—Average bump heights on various chip positions when deposited from sulfonate bath at 30 mA/cm^2 for different electrodeposition times.

Acknowledgment

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