Circuit Technology

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New Approach to PWB Construction

Printed circuit fabrication has evolved over the past half-century from a very crude early print-and-etch technique to an extremely sophisticated manufacturing process. The initial evolution began with plated through-hole copper metallization, which allowed an electrical connection between both sides of a printed wiring board (PWB) and enabled insertion mount components to be more securely bonded. Thereafter, techniques were developed to permit internal wiring for multilayer PWBs.

Multilayer printed circuits were popular in military and high-tech commercial circuits during the 1970s. The decline of single- and double-sided PWBs and the dramatic increase of multilayer PWBs in the '80s was a direct result of the success of surface mount technology.

Based Sales of PWBs Produced in the U.S., %[1]

PWB Type	1980	1985	1990	1995
Single-sided glass	14.9	9.8	8.1	6.0
Double-sided	49.9	31.1	23.5	20.2
Flex/rigid flex	5.6	7.5	6.6	6.6
Multilayer	29.6	51.6	61.8	65.2
Total	100.0	100.0	100.0	100.0

Surface Finishes on PWBs, %[1]

Surface Finish	1994	1995	1996	1997	1998
HASL	71.9	75.3	74.6	59.7	56.8
Re-flowed Sn/Pb	10.0	5.2	5.3	5.0	3.6
Total fused Sn/Pb	81.9	80.5	79.9	64.7	60.4
(OSP)	12.7	15.9	12.5	28.2	30.0
Ni/Au-Ni/Pd	3.9	1.6	6.1	6.8	9.1
Other	1.5	2.0	1.5	0.3	0.5
Total	100.0	100.0	100.0	100.0	100.0

Keeping Up With Advancements In Semiconductor Technology

The past 10 years witnessed lighter, smaller and denser interconnections—vital for speed and heightened signal integrity to maximize benefits of *avant-garde* semiconductor technology. The driving force is increased integration of transistors into semiconductor die. To accommodate more functions on the (same-sized) silicon real estate, a large increase in I/Os is required. A major advantage is higher speed in circuit switching.

Printed circuit board assemblers are employing innovative bonding techniques to improve efficiency and reliability of components with greater than 200 I/Os. These include wire bonding, tape automated bonding (TAB), ball grid array (BGA), flip chip, micro ball grid array (MBGA), tape ball grid array (TBGA) and direct chip attachment (DCA).

Extensive use of ultra-fine pitch components coupled with advanced bonding techniques has placed a limitation on fused tin/lead, which had been the preferred surface finish. This change came in 1997 as OSPs and precious metal finishes replaced HASL in high-density circuitry.

Microvia Buildup Technology

To further magnify interconnect density, thinner PWBs with buried and blind microvias and narrower lines/spaces are pivotal. Standard drilling technology can facilitate a via pad size of 635 microns (25 mil) with a 381-micron (15 mil) hole. Cost rises significantly as smaller hole size is exacted. A via of 203 microns (8 mil) appears to be the practical limit, but even that level may augment a PWB price by as much as 30 percent. Also, as the hole size becomes smaller for the same thickness board, the aspect ratio increases. High-aspect ratio holes tend to decrease reliability as a result of plating and solder hole fill problems. To form small vias, methods other than mechanical drilling are used (laser, plasma, photochemical), leading to a new approach to multilayer manufacturing: "buildup technology."[3]

Currently, 60 companies worldwide are using 20 different processes to achieve higher density interconnection. Products where miniaturization provides a vital competitive advantage (cell phones, notebook computers, cam-corders, pagers) are consuming the limited availability of these PWBs.[4]

The reason for the limited supply of these high-density interconnection structures (HDIS) is that PWB manufacturers are reluctant to expand capacity until they can refine techniques for registration, fine-line lithography, metallization and plating, and determine the best approach to via formation (laser, plasma or photo).

This technology not only has the potential to satisfy the industry's future performance needs, it also has a cost-effective potential over current procedures. Paramount is production experience to refine techniques to guide PWB manufacturers to the most economical process for equipment investment so that anticipated demand for microvia buildup technology can be satisfied. P&SF

References

1. IPC Technical Marketing Research Council data.
2. Coombs, C., *Printed Circuit Handbook*, Ch. 9.4, McGraw Hill, 4th ed., 1995.
3. Dwyer, H.E. "Advanced Electronic Interconnect—Cost and Opportunities," *Proceedings NEPCON West*, 1998.
4. Holden, H., "High Density Interconnect Substrates." *Board Authority*, Vol. 1, No. 2, A Supplement of *Circuitree*, June 1999.