Electrically Mediated Plating of Semiconductor Substrates, Chip Scale Packages & High-density Interconnect PWBs

By E.J. Taylor, J.J. Sun, B. Hammack, C. Davidson & M.E. Inman

This paper describes a process for low-cost plating of electronic interconnects for integrated circuits (IC), chip scale packages (CSP), and high-density interconnect printed wiring boards (HDI-PWB). In contrast to traditional chemical mediation of plating processes, the electrically mediated process does not rely on difficult-to-control leveling additives, such as brighteners and/or levelers. The methodology for selection of the electric mediation parameters is based on an understanding of the interactions of an "electrodynamic diffusion layer" with microprofiles and macroprofiles to control the metal distribution. Data for plating of sub-micron trenches, 30 to 75 micron microvias, and high-aspect-ratio PTHs is presented. In addition to simplicity and robustness of the electrically mediated approach, data demonstrating the ability to metallize and planarize with minimal overplate is presented. The ability to plate/planarize is important for: (1) reducing or eliminating chemical mechanical polishing of ICs, (2) fabricating stacked microvias for CSPs, and (3) fine-pitched interconnects for HDI-PWBs.

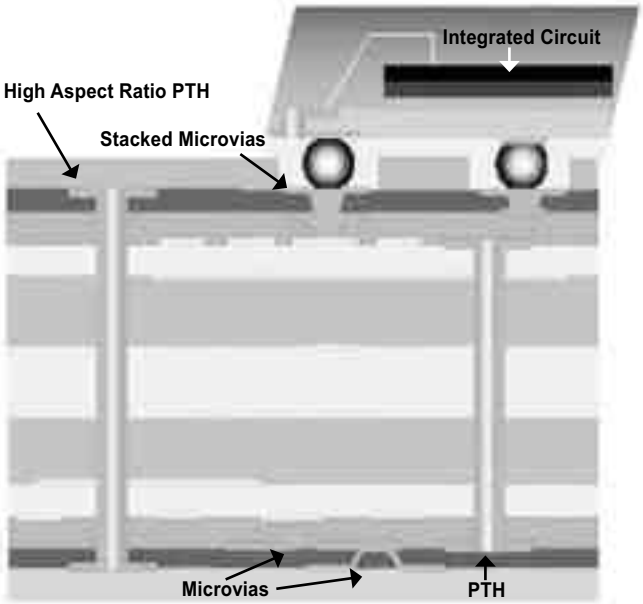

Fig. 1—Schematic of advanced electronic package.

The continuing trend toward miniaturization of consumer electronics is presenting considerable technological challenges to all segments of the electronics industry. Specifically, in advanced integrated circuits (ICs), copper interconnections are replacing aluminum.[1,2] Because the performance capabilities and miniaturization of IC devices are proceeding at a rate significantly faster than the printed wiring board technology required to interconnect them,[3] the need for chip scale packages (CSPs) and high-density interconnect printed wiring boards (HDI-PWBs) has emerged. As depicted in Fig. 1, the CSP and HDI-PWB provide the z-axis interconnection between the IC and the PWB.

The challenge of plating electronic interconnects is one of leveling or throwing power (*i.e.*, the uniform deposition of a conductor into microprofiles[4]). There are two types of leveling: geometric leveling and true leveling.

Geometric leveling results from a uniform or primary current distribution. Consequently, the plating rate must be very slow. Geometric leveling only occurs when the deposit is at least as thick as the depth of the microprofile, so the overplate is considerable. Geometric leveling is impractical for fabrication of electronic interconnects.

True leveling results from the preferential adsorption of a specific leveling additive or additives on the high-current-density areas (*e.g.*, peaks or corners of the microprofile). True leveling requires precise control of these additives, also known as levelers and brighteners.

In conventional direct-current (DC) plating of plated through-holes (PTHs) for the PWB industry, leveling additives are incorporated in the plating bath to improve the throwing power and to yield a fine-grained deposit.[5,6]

Nuts & Bolts: What This Paper Means to You

Features on printed wiring boards (PWBs) and interconnects are getting smaller and smaller . . and smaller. Maintaining uniformity and leveling in copper plating of these tiny features with the tools we have is getting harder and harder . . and harder. Interest in pulse plating and all of its variations is getting more intense by the day. Here, the authors consider just what pulse can do in meeting the demands of today's PWB designs.

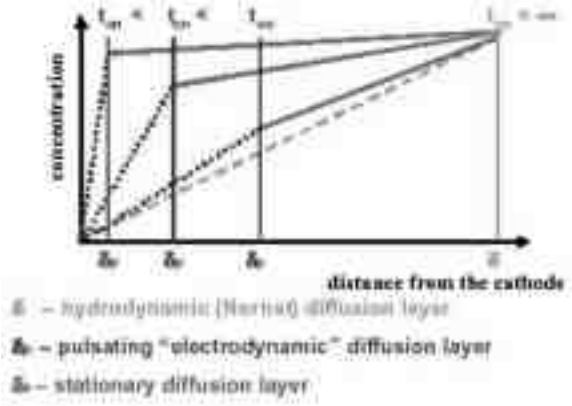

Fig. 2—Schematic representation of diffusion layer.

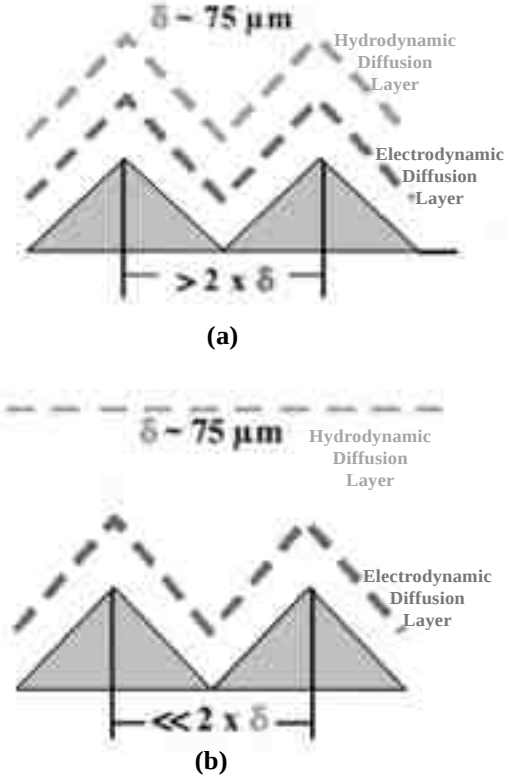

Fig. 3—Relationship between the hydrodynamic diffusion layer and the electrodynamic diffusion layer for (a) macroprofile and (b) microprofile.

Considerable challenges exist, however, for extension or insertion of PTH electroplating processes to the smaller microvias and IC features. Specifically, the proprietary chemistries used in "conventional" and "high-throw" baths do not necessarily provide acceptable results for smaller interconnect features,[7] and proprietary chemical formulations must be optimized for different feature sizes.[8] Furthermore, bath maintenance and control issues associated with the leveling additives are exacerbated at HDI, CSP and IC feature sizes.

To meet the plating challenge of advanced electronic interconnects, non-DC plating processes have recently received considerable interest.[9-13]

While these non-DC processes have been referred to by a variety of names (*e.g.*,periodic reverse plating and pulse reverse plating), they all utilize brighteners and/or levelers and are, therefore, a form of true leveling.

Consequently, the challenge of precise control of leveling additives remains. In addition, these previous studies[9-13] have used one

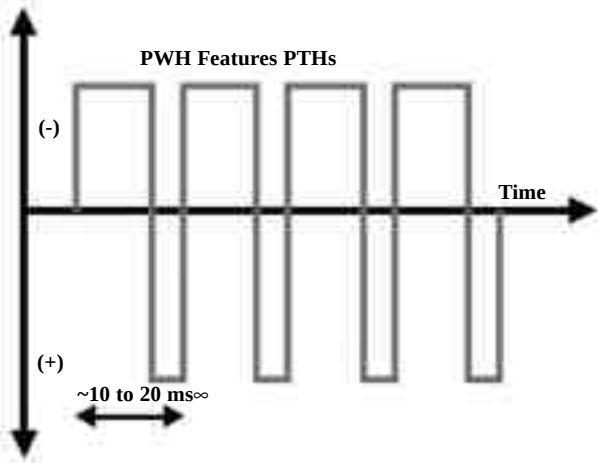

Fig. 4—Generalized waveform for PTH.

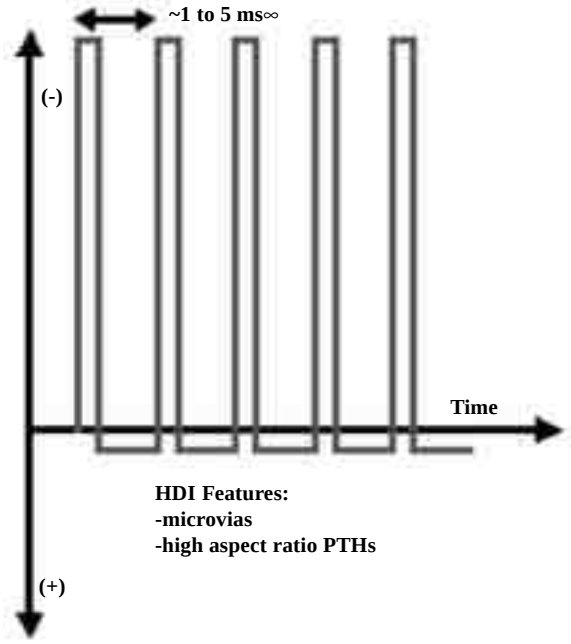

Fig. 5—Generalized waveform for high-aspect-ratio PTHs and microvias.

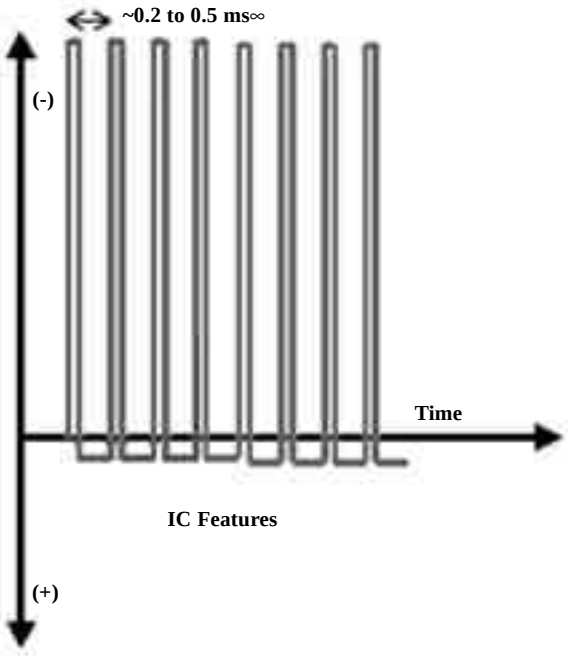

Fig. 6—Generalized waveform for IC features.

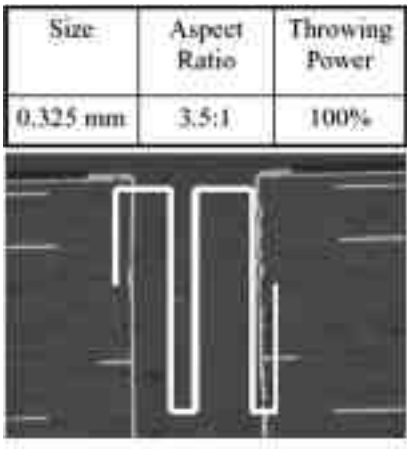

Fig. 7—Electrically mediated plating of PTH.

set of waveform parameters, characterized by a long forward or cathodic pulse followed by a short reverse or anodic pulse.

As suggested from fundamental considerations, however,[14] changes in waveform parameters should have a substantial impact on the copper plating of interconnect features. In addition, Rehrig and Mandich[15] studied the effect of pulse plating parameters on throwing power. They suggested that "simple electronic manipulation of the pulse waveform" could be used to "tune" the electrodeposition process and replace the complicated brightener/leveler chemistries.

Recently, copper plating for electronic applications without brighteners and levelers has been reported.[16-18] This process is termed *electrically mediated copper plating*, in contrast to the conventional chemically mediated approach using leveling additives. In this paper, we present further results using electrically mediated copper plating of electronic interconnects.

Approach

In the electrically mediated approach, the forward on-time/peak current and reverse on-time/peak current are tuned to plate specific electronic features. The rationale for selecting the process parameters is derived from the influence of a pulsating current on the hydrodynamic diffusion layer. As shown in Fig. 2, during pulse plating, a "duplex diffusion layer" develops. The duplex diffusion layer consists of a stationary layer and an inner pulsating layer. By assuming linear concentration gradients, Ibl[19,20] derived the following relationship between the pulsating diffusion layer and the on-time of the pulse:

$$\delta_p \approx (2Dt_{on}) \quad (1)$$

where D is the diffusion constant, t_{on} is the on-time of the pulse and δ_p is the pulsating diffusion layer. More recently, using a similar duplex diffusion layer approach, the same relationship was derived for "pulse-with-reverse" plating.[21] Because the pulsating diffusion layer is determined by the on-time of the pulse, we refer to it as the "electrodynamic diffusion layer."

As shown in Fig. 3, proper selection of the electrodynamic diffusion layer can convert a macroprofile to a smaller macroprofile or convert a microprofile to a smaller microprofile. In order for diffusion processes and thereby the electrodynamic diffusion layer to influence the plating process, however, mass transport effects must be significant during the duration of the pulse. The time required for the concentration of reacting species at the interface to be depleted to zero is known as the transition time, τ, and is given by the Sand equation:

$$\tau \approx ((nF)^2 C^2 D)/2i_{on}^2 \quad (2)$$

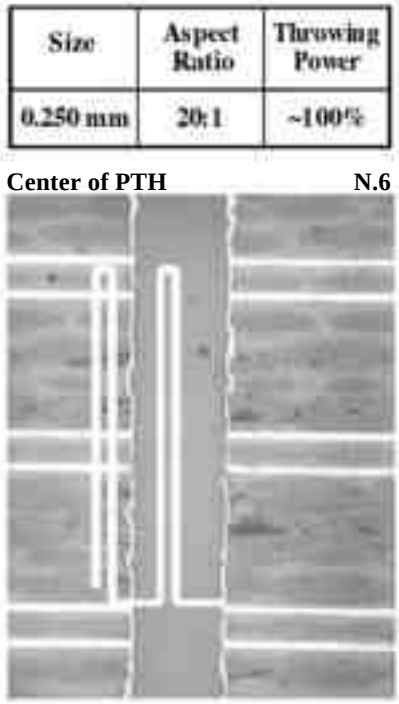

Fig. 8—Electrically mediated plating of high-aspect-ratio PTH.

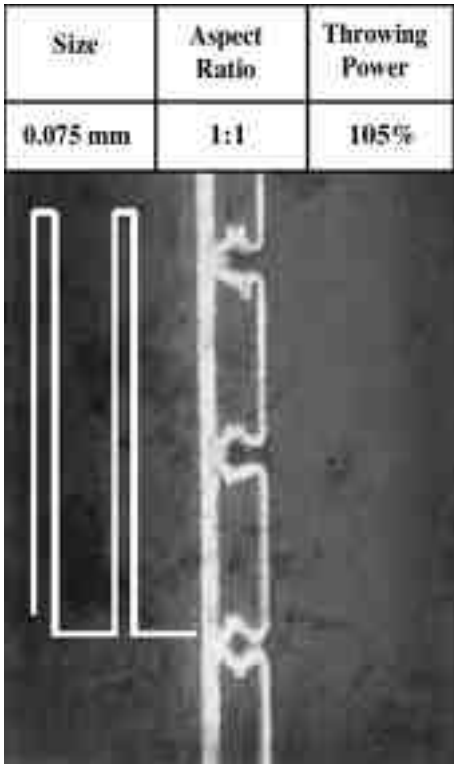

Fig. 9—Electrically mediated plating of microvias for HDI-PTH.

where n is the number of electrons, F is Faraday's constant, C is the bulk concentration of the reacting species, and i_{on} is the pulse current. Consequently, mass transport effects influence the plating process when the transition time is significantly less than the on-time:

$$\tau << t_{on} \quad (3)$$

While the theoretical framework is not sophisticated enough to allow *a priori* determination of waveform parameters, the above

discussion and previous work[16-18] provide substantial guidance. Specifically, low-aspect-ratio PTHs are macroprofiles and require a relatively long forward on-time followed by a relatively short reverse on-time. The sum of the forward on-time and reverse on-time, as well as any off-times, is approximately 10 to 20 msec, or 100 to 50 Hz. The general form of the electrically mediated process waveform for PTHs is presented in Fig. 4.

High-aspect-ratio PTHs, microvias, and IC features are microprofiles and require short forward on-time/high forward peak current, followed by a relatively long reverse on-time/low reverse peak current. For high-aspect-ratio PTHs and microvias, the sum of the forward on-time and reverse on-time, as well as any off-times, is approximately 1 to 2 msec, or 1000 to 500 Hz. For IC features, the sum of the forward on-time and reverse on-time as well as any off-times, is approximately 0.2 to 0.5 msec, or 5000 to 2000 Hz. The general form of the electrically mediated process waveforms for high-aspect PTHs/microvias and IC features are presented in Figs. 5 and 6, respectively.

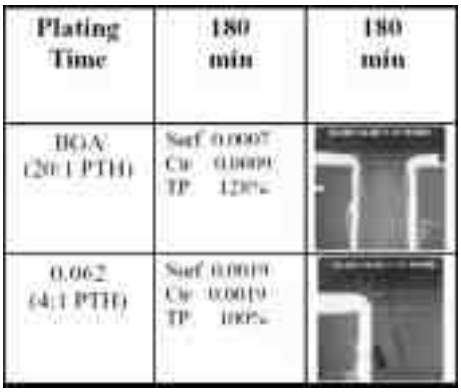

Fig. 10—Electrically mediated plating of high-aspect-ratio BGA and low aspect ratio PTH.

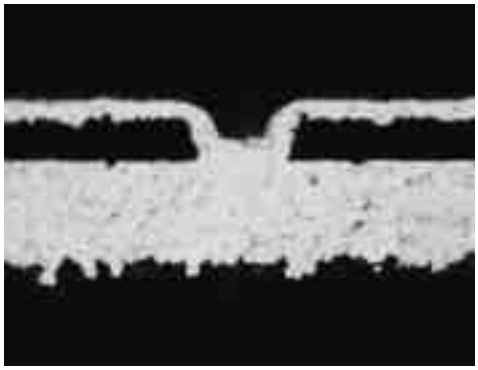

Fig. 11—Electrically mediated plating of 30 mm microvia for CSP.

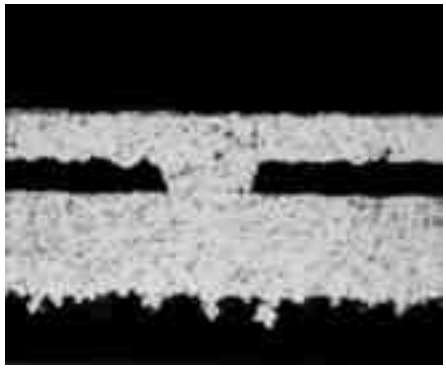

Fig. 12—Electrically mediated plating of 30 mm microvia for CSP, with process parameters adjusted to fill microvia.

Experimental Procedure

An acid copper sulfate solution containing 60 g/L $CuSO_4$, 9% by volume of H_2SO_4, 60 ppm Cl^-, and 350 ppm polyethylene glycol (PEG) was used as the copper electroplating bath for all experiments. The chloride/PEG acts as a suppressor and is not difficult to control.[22] The plating bath does not contain difficult-to-monitor/control additives such as brighteners and/or levelers. The plating bath temperature was 25°C (78°F).

For the HDI-PWB features, plating experiments were conducted on 20.3 x 45.7-cm (8 x 18 in.) panels of 0.318 and 0.635 cm (0.125 and 0.250 in.) thicknesses containing microvias, PTHs and ball grid arrays (BGAs). The plating line (vertical) consisted of a single panel flight bar with eductors oriented at 90° perpendicular, knife-edge agitation and mesh insoluble anodes. As described previously, the insoluble anodes offered potential advantages for reverse pulse plating.[23] For the CSP and IC features, plating experiments were conducted on 1.9 x 1.9 cm (0.75 in.) samples in a rotating electrode apparatus.

Results

In Fig. 7, the results for the electrically mediated copper plating of a 3.5:1 aspect ratio PTH are presented. The waveform used was the long forward on-time/short reverse on-time at a frequency of approximately 50 Hz. The throwing power was approximately 100 percent.

In Fig. 8, the results for the electrically mediated copper plating of a 20:1 high-aspect-ratio PTH are presented. The waveform used was the short forward on-time/long reverse on-time at a frequency of approximately 500 Hz. The throwing power was approximately 100 percent. Further optimization of the electrically mediated process parameters is expected to yield the desired throwing power.

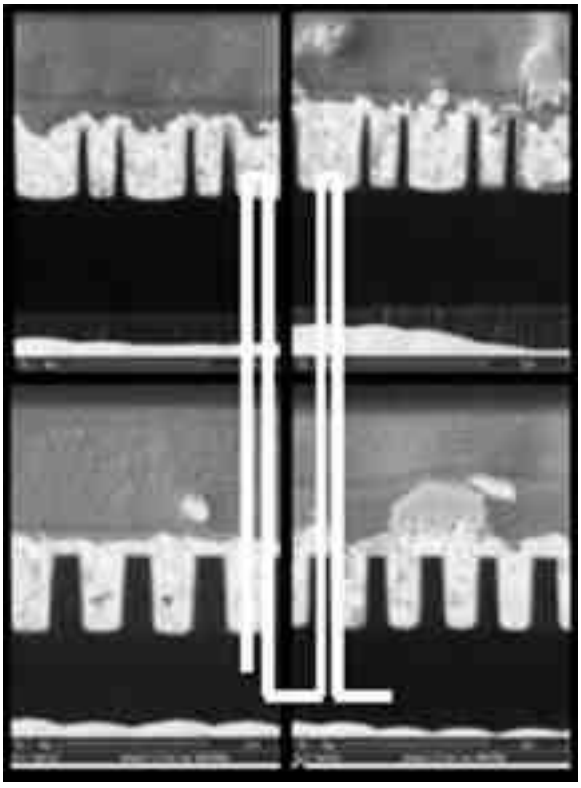

Fig. 13—Electrically mediated plating of 0.25, 0.50 and 0.77 mm IC feature.

In Fig. 9, the results for the electrically mediated copper plating of microvias for HDI-PWBs are presented. The waveform used was the short forward on-time/long reverse on-time at a frequency of approximately 500 Hz. The throwing power was approximately 100 percent.

In Fig. 10, the results for the electrically mediated copper plating of an HDI-PWB containing a high-aspect-ratio BGA and a low-aspect-ratio PTH are presented. The excellent throwing power and coverage results were obtained using the long forward on-time/short reverse on-time at a frequency of approximately 50 Hz followed by the short forward on-time/long reverse on-time at a frequency of approximately 500 Hz.

In Fig. 11, the results for the electrically mediated copper plating of microvias for CSPs are presented. The waveform used was the short forward on-time/long reverse on-time at a frequency of approximately 2000 Hz. The throwing power was approximately 100 percent. In Fig. 12, the process parameters were adjusted to fill the microvia. The ability to fill microvias is important to enable the stacked microvia designs illustrated in Fig. 1.

In Fig. 13, the results for the electrically mediated copper plating of IC features are presented. Good void-free filling for 0.25, 0.50 and 0.77 µm IC features are obtained. Of particular note is the minimal overplate associated with the electrically mediated process.

Summary

An electrically mediated process for copper plating of electronic interconnects is described.[24,25] Specifically, copper plating PTHs and microvias for HDI-PWB, microvias for CSP and IC features ranging in size from 325 down to 0.25 µm. In contrast to conventional plating art based on brightening/leveling additives, the electrically mediated process is based on predictable knowledge.

The critical parameters of the electrically mediated process are forward and reverse on-times and forward and reverse peak currents. By understanding the influence of an electrodynamic diffusion layer on macroprofiles and microprofiles, the process parameters are tuned to the electronic interconnect feature of interest. As additional knowledge and experience is derived from the electrically mediated process, a library of process parameters will be developed. Consequently, as new electronic packages are required, the electrically mediated process parameters will be selected from a library of process parameters.

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