

A Low Cost Semiconductor Metallization/Planarization Process

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This paper presents an electrically-mediated process for copper metallization of semiconductor interconnect features. Compared to traditional metallization processes, the proposed electrochemical deposition process uses a single-component bath that contains no difficult-to-control organic accelerators and levelers. The feasibility of the process is demonstrated by copper deposition onto sectioned VLSI wafers. Focus ion beam scanning electron microscopy (FIB-SEM) pictures of metallized interconnect features are presented for feature sizes in the range of 0.25 to 10 μm (~10 to 400 $\mu\text{-in.}$).

For the past four decades, the semiconductor industry has continued to improve semiconductor devices in order to comply with the market demand for higher performance, cost-effective products. The continued decrease of feature sizes on integrated circuits (IC) has increased circuit performance and yield at a lower cost per function on chips.

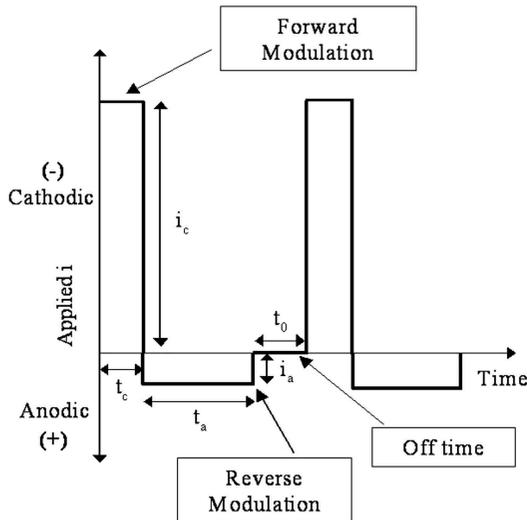
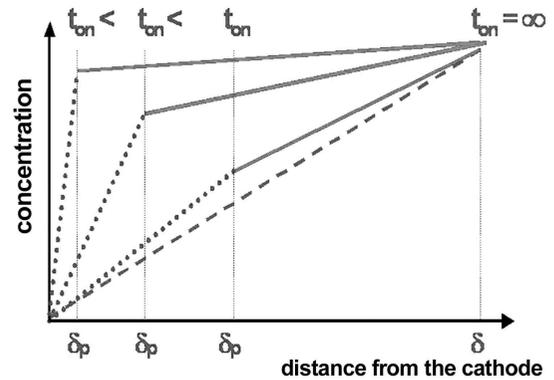


Fig. 1—Electrically-mediated waveform.

Nuts & Bolts: What This Paper Means to You

Electrically-mediated plating voltage techniques offer potential cost reductions in fabricating semiconductor interconnect features. This work has shown the possibility of obtaining interconnect features in the 0.25 to 10 μm range from a single-component copper bath with no organic additives. Such methods offer considerable promise for manufacturing such small-scale features.



δ – hydrodynamic (Nemst) diffusion layer
 δ_p – pulsating “electrodynamic” diffusion layer
 δ_s – stationary diffusion layer

Fig. 2—Schematic representation of diffusion layers.

According to the Semiconductor Industry Association (SIA), the reduction in feature size is approximately 30% every three years.¹ However, as feature sizes shrink into the submicron region (<0.25 μm ; 10 $\mu\text{-in.}$), the resistance-capacitance (RC) delay associated with the interconnect features becomes the dominant performance limiting factor. The RC delay results from an increased resistance arising from the narrowing of the interconnections and an increased capacitance arising from the closer proximity of the interconnections. An increase in the RC delay has a negative impact on the speed and power consumption of IC devices.

Originally metal interconnects on IC devices were fabricated from aluminum and aluminum alloys, since aluminum has a relatively low electrical resistance and can be easily deposited and etched. However, as feature sizes were reduced, it became apparent that aluminum was unable to conduct the necessary current reliably in order to maintain or increase IC performance. To compensate for this problem, the semiconductor industry began investigating the use of copper as a replacement for aluminum as the conductor on IC devices, and in 1997 IBM announced the integration of copper chip technology into its products.²

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Compared to aluminum, the implementation of copper into IC devices has several notable advantages that make it attractive for metallization of interconnect features:^{3,5}

- lower electrical resistance
- higher electromigration resistance
- higher thermal conductivity
- higher reliability
- low cost
- proven deposition methods

The lower electrical resistance of copper decreases the RC delay and produces higher currents at a given voltage enabling the production of faster, denser chips with increased computing power. In addition, the lower resistivity of copper reduces the necessary number of interconnect levels, which drastically decreases the number of processing steps, thus reducing processing costs.⁵

The switch from aluminum to copper for metallization of interconnect features has also resulted in a decrease in electromigration, a phenomenon identified as one of the primary failure mechanisms limiting IC reliability. Electromigration occurs when mobile electrons responsible for the electrical current within the circuit collide with stationary atoms, causing diffusive transport of these atoms in the direction of the electron flow. As a result, the metal thins in one area of the interconnect while accumulating in another area, initiating electrical failure of the IC.⁴ The higher electromigration resistance of copper increases the reliability of the IC for a given interconnect design.

Aluminum interconnects are fabricated by conventional sputter deposition and reactive ion etching (RIE) techniques. Copper is not easily etched by conventional RIE because of the lack of volatile by-products. Therefore the aluminum-to-copper conversion in the semiconductor industry required the development of new methods for the metallization of interconnect features. Several techniques have been investigated for filling interconnect features with copper, including physical vapor deposition (PVD), chemical vapor deposition (CVD), electroless plating and electrochemical deposition (ECD).^{5,8} The most common technique currently utilized for fabrication of IC devices by the semiconductor industry is the Damascene process, which utilizes ECD for depositing the copper onto IC devices.

The Damascene process, developed by IBM, involves etching a pattern of interconnect features, *i.e.*, trenches and vias, in a dielectric film, then filling the pattern with copper using ECD techniques. Before depositing the copper, a barrier layer is applied to prevent the copper from diffusing into and poisoning the dielectric material. Additionally, a small copper seed layer is deposited using a non-electrolytic process, such as PVD, prior to complete filling of the interconnect features with copper using ECD. The seed layer is necessary to ensure good electrical contact to all areas of the wafer where copper deposition is desired during the ECD process. The main problems associated with ECD of copper interconnect features are the filling of submicron, high-aspect-ratio vias and trenches without void or seam formation and copper overfill on the wafer surface.

The formation of voids and seams can occur because the size and geometry of the trenches and vias makes the bottoms of these

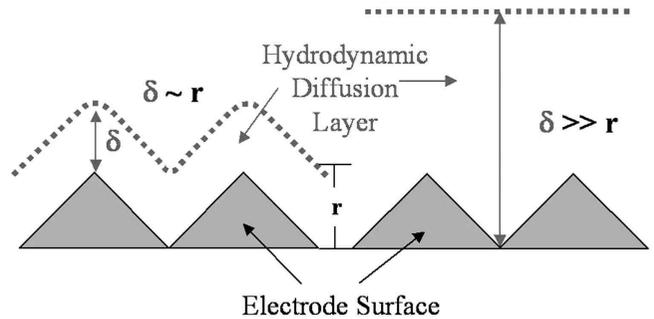


Fig. 3—Macroprofile (left); microprofile (right).

features less accessible to copper during the seeding and filling process. These defects can ultimately lead to failure of the IC component. To avoid defects initially during the filling process, the seed coverage must be smooth and continuous over the entire feature. Once an optimal seed layer has been deposited, the trench or via can be filled with copper using ECD. Different filling profiles have been described,⁹ and superfilling, *i.e.*, the filling of trenches and vias from the bottom up, is currently the most accepted profile for producing defect-free submicron features.

Superfilling occurs due to increased deposition rates along the sides and bottom of the trenches and vias. This is usually achieved by passing direct current (DC) through a copper plating solution containing two types of organic additives, accelerators and suppressors. In these two-component baths, the suppressors are large organic molecules that bind the copper at the surface of the wafer to minimize copper deposition there. The molecules are too large to fit inside the submicron features and thus do not affect the deposition of the copper inside the features. Polyethylene glycol (PEG) is an example of a suppressor and chloride is often added to copper plating baths as a co-suppressor. The accelerators are typically small organic molecules that are capable of fitting into the interconnect features and enhancing the deposition rate of the copper inside the features. As the submicron features are filled, the accelerator molecules remain concentrated over the smaller interconnect features creating bumps that lead to an uneven copper film on the wafer surface.¹⁰ The uneven copper distribution on the surface of the wafer creates challenges for subsequent processes, such as chemical mechanical planarization (CMP), required to remove the copper overfill so that the interconnect can be integrated into a multi-level metallization package.

To prevent the bump that results from superfilling, a third component, a leveler, can be added to the plating bath. However, studies have shown that in three-component baths high leveler concentrations initiate voids in the interconnect features and low leveler concentrations do a poor job of minimizing the copper bump over the smaller features.¹¹ The process can be separated into a two-step

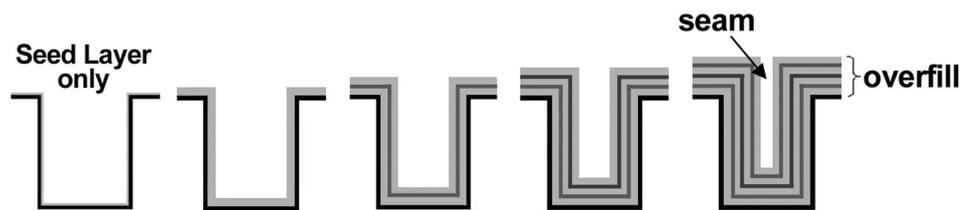


Fig. 4—Conformal filling profile during PC process.



Fig. 5—Novel filling profile for electrically-mediated process. The first picture shows the initial seed layer. This is followed by the conformal deposition of copper. Next the preferential etching of the upper sidewalls and re-entrant of interconnect feature is shown. The final result is a void-free copper filled feature with minimal overfill and a planarized surface.

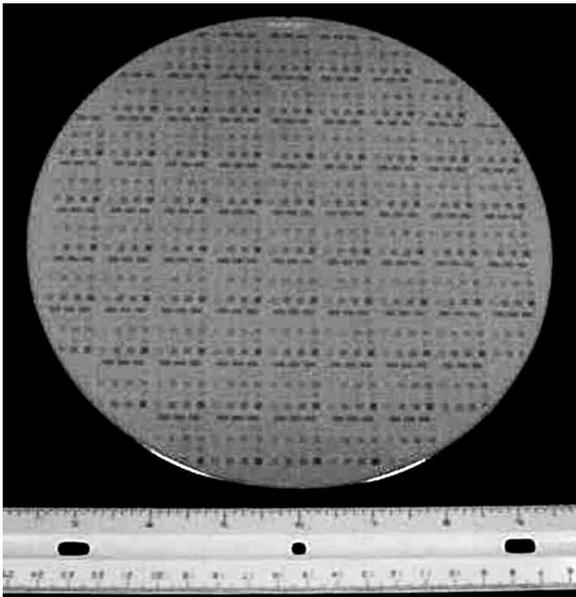


Fig. 6—200-mm wafer before being sectioned into 19 x 19 mm test coupons.

process where the first step focuses on defect free filling of features from a bath containing the accelerators and suppressors and the second step focuses on planarization of the copper on the surface of the wafer using a bath that contains the leveler. Although this two-step process has been successful, it adds additional processing time and costs.

Although the previously mentioned organic additives help to eliminate defects in the filling process, they create additional problems. Since copper reacts with most levelers, the incorporation of additives results in a brittle and highly resistive copper deposit,¹² which negatively impacts the performance of electrical devices. Experimental results by Chang and coworkers have demonstrated that interconnect features plated with copper in the absence of additives exhibit a lower resistivity compared to those plated under the same conditions in the presence of additives.¹³ Additionally, since the additives are slowly incorporated during the deposition process, and since research in modeling has shown that the smallest imbalance in the system can create defects in the trenches and vias,¹⁴ it is necessary to monitor the precise concentration of the additives closely. The monitoring equipment can be expensive to purchase and maintain, thus increasing the cost of the manufacturing process.^{**} Moreover, different feature sizes require different amounts of chemical additives for defect-free filling of trenches and vias.¹⁶ Consequently, IC devices with multiple interconnect features must go through a series of steps, involving the changing of plating baths and the masking of previously plated features to produce desired deposit characteristics (*i.e.*, throwing power, con-

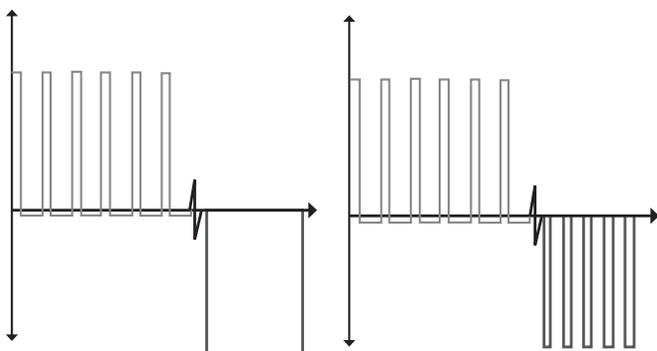


Fig. 7—Schematic of experimental waveforms with DC etch (left) and electrically-mediated etch (right).

ductivity, etc). For these reasons, it is necessary to develop filling processes that substantially reduce or even eliminate the need for organic additives in plating solutions.

Electrically-mediated processes are being investigated as alternatives to the conventional DC processes used for ECD of copper interconnect features.¹⁷⁻²¹ Compared to DC plating, electrically-mediated processes present several potential advantages, such as reduction in plating time and waste, improved deposition properties, higher current efficiency and the reduction of additives.^{22,23} In addition, when optimized for specific features, electrically-mediated waveforms have the ability to completely fill vias and trenches with substantially less copper overfill and a more planar surface. In most processes currently used for production, anywhere from 0.5 to 1.5 μm (~20 to 60 $\mu\text{-in.}$) of copper overfill needs to be removed to leave only the trenches and vias embedded in the dielectric material.²⁴ It is estimated that the CMP process generates between 30 and 50 L (4.0 to 6.7 gal) of waste slurry per 20.3-cm (8.0-in.) wafer.²⁵ Reducing the copper overfill on the wafer surface could significantly reduce the CMP time and slurry waste, thus reducing manufacturing costs.

In the electrically-mediated process, we use a single-component copper plating bath containing only the suppressor additive, PEG. For reasons mentioned previously, this is not considered a “difficult-to-control” additive. With the electrically-mediated process, different feature sizes can be filled in the same process step by waveform sequencing, the copper overfill is minimized and the surface made more planar by controlling and optimizing the applied waveform instead of the plating chemistry. This yields a process that is inherently easier to control while reducing the manufacturing time by reducing the number of processing steps, all of which could potentially lead to a reduction in the manufacturing costs.

Approach

Electrically-mediated waveforms have the potential to significantly enhance ECD processes by optimizing the associated process parameters shown in Fig. 1. Additional parameters include the cathodic duty cycle, γ_c , and the anodic duty cycle, γ_a , which are the ratios of the respective pulse on-times to the period and are used to calculate the average current density (i_{avg}):

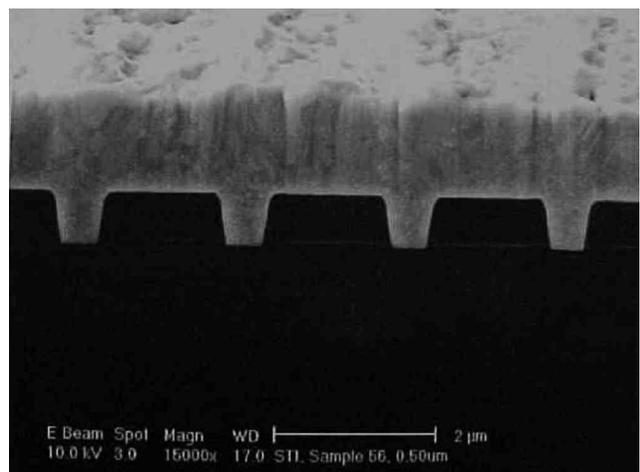


Fig. 8—0.5- μm lines filled with electrically-mediated waveform in the absence of an etching period.

^{**} It should be noted that studies¹⁵ have shown the PEG additive concentration can vary substantially from the optimal concentration without affecting the filling of the interconnect features, therefore the PEG additive is not considered “difficult-to-control” in terms of concentration and does not need to be as closely monitored as the other additives.

$$i_{\text{aver}} = i_c \gamma_c - i_a \gamma_a \quad (1)$$

In ECD processes the current density is limited by the diffusion of the ions to the electrode surface, which is related to the thickness of the diffusion layer. In a DC process, the hydrodynamic diffusion layer, γ , establishes the current density.

Previous work^{26–30} has shown that during electrically-mediated processes, a “duplex diffusion layer” is established, incorporating both a stationary layer, γ_s , and a pulsating layer,³¹ γ_p , also referred to as the electrodynamic diffusion layer (Fig. 2). Assuming a linear concentration gradient across the electrodynamic diffusion layer, the thickness of γ_p is described by the following equation:²⁷

$$\gamma_p = (2Dt_{\text{on}})^{1/2} \quad (2)$$

where D is the diffusion coefficient of the reacting species and t_{on} is the pulse on-time.

In order for the electrodynamic diffusion layer to influence the deposition process, the mass transport effects must be significant during the pulse on-time. This occurs when the reacting species at the electrode/solution interface is exhausted and must be replenished by ions diffusing to the electrode. The time it takes for the reacting species to be depleted at the interface is referred to as the transition time, τ , and is defined by Equation (3):

$$\tau = \frac{\Pi(nF)^2 C_b^2 D}{4i_c^2} \quad (3)$$

where n is the number of electrons transferred, F is Faraday’s constant and C_b is the bulk concentration of the ions being deposited. Therefore, mass transport effects only strongly influence the electrochemical deposition process when t_{on} is much larger than τ .

In ECD processes, mass transport effects produce two distinct situations. The first situation, shown on the left in Fig. 3, is referred to as a macroprofile case. In a macroprofile, the surface roughness is large compared to the thickness of the diffusion layer, and the diffusion layer tends to follow the surface contour. Under mass transport or diffusion control, a macroprofile results in a uniform current distribution and a conformal deposit or etch, depending on whether a forward or reverse pulse is applied.

In the second situation, the surface roughness is small compared with the thickness of the diffusion layer. This results in a microprofile case shown on the right in Fig. 3. Under mass transport control, a microprofile results in a non-uniform current distribution and preferential deposition or etching.

Since the thickness of the diffusion layer under conditions of moderate bath agitation is on the order of $75 \mu\text{m}$ ($\sim 300 \mu\text{-in.}$), and the vias and trenches are less than $1 \mu\text{m}$ ($\sim 4 \mu\text{-in.}$), the filling of the trenches and vias fits a microprofile case. For void-free copper deposition into trenches and vias, the optimum waveform should uniformly deposit copper during the cathodic modulation. To ensure uniform deposition of the copper into the trenches and vias, the waveform parameters are chosen so the microprofile is converted into a macroprofile during the cathodic modulation.

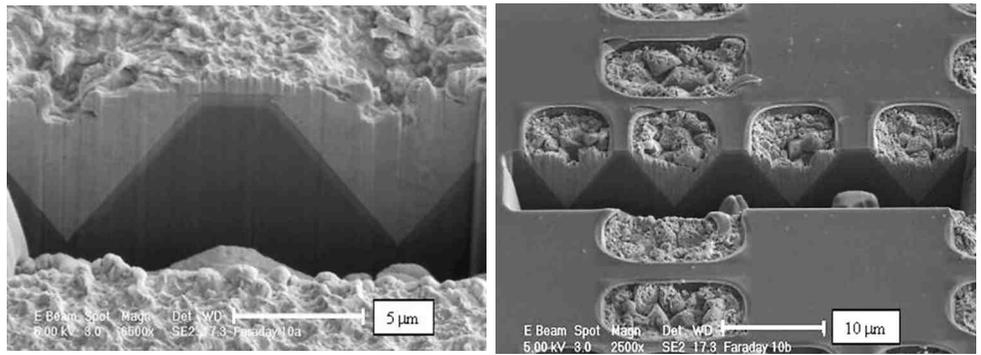


Fig. 9— $8\text{-}\mu\text{m}$ trenches filled with copper using an electrically-mediated waveform and no etch period (left) and $8\text{-}\mu\text{m}$ trenches filled with copper using electrically-mediated waveform followed by an electrically-mediated etch period.

This can be achieved by using a high cathodic peak current for a relatively short on-time. These parameters can be rationalized by examining Equation (2) and Equation (3). To convert from a microprofile to a macroprofile, the diffusion layer thickness must be decreased. According to Equation (2), the diffusion layer is proportional to the on-time, so a short on-time will produce a thin diffusion layer. Also, for mass transport effects to be significant, the transition time, τ , must be much smaller than the on-time, t_c . Equation (3) shows that the transition time is inversely proportional to the cathodic peak current, so a large cathodic peak current will yield a short transition time. In the case of a macroprofile, copper deposition will be conformal, however, conformal filling profiles often produce seams in trenches and vias and result in significant overfill as shown in Fig. 4.

The addition of an anodic modulation eliminates defects and reduces overfill by conformally depositing copper during cathodic modulation and preferentially etching copper from the surface, re-entrant and upper sidewalls of the trenches and vias during the anodic modulation. This promotes planarization of the surface during the filling process with minimal copper overfill.

This is achieved by using the high cathodic peak current for a short on-time during deposition, then creating a non-uniform current distribution during the etch process using a low anodic peak current for a relatively long on-time. Again, the choice of these parameters can be justified with Equation (2) and Equation (3).

Figure 5 shows a schematic of the proposed filling profile. The filling profile begins by showing the interconnect feature prior to ECD, containing only the seed layer. Next the conformal deposition process is shown, followed by the feature after etching. The final result of this filling profile is a planarized, defect-free copper

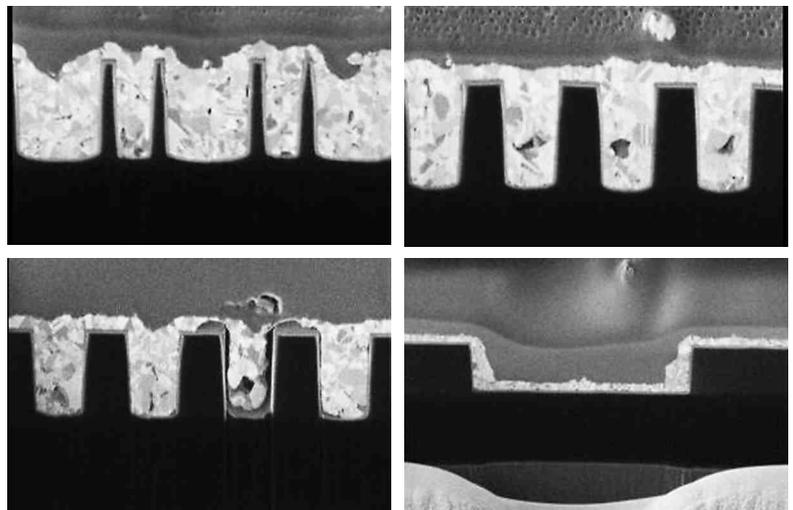


Fig. 10—FIB-SEM cross section of trenches and vias filled using an electrically-mediated waveform with an electrically-mediated etch: (a) Via chain, $0.25\text{-}\mu\text{m}$ lines, $0.50\text{-}\mu\text{m}$ holes; (b) Trench, $0.77\text{-}\mu\text{m}$ lines; (c) Trench, $0.96\text{-}\mu\text{m}$ lines; (d) Trench, $9.96\text{-}\mu\text{m}$ lines.

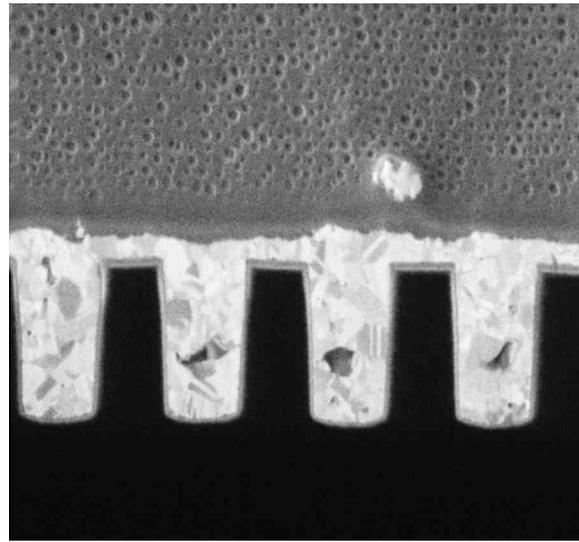
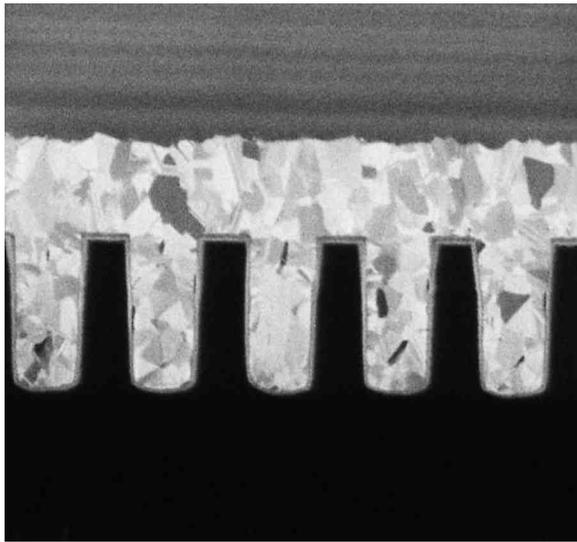


Fig. 11—0.77- μm line filled with electrically-mediated waveform and electrochemically leveled with DC (left) and electrically mediated current (right).

filled trench or via with considerably less copper overfill than trenches and vias filled by processes that follow conformal or superfilling profiles.

It has been shown that the electric field effects cannot be responsible for the uneven current distributions, since the ohmic drop in the plating solution is negligible at the scale of the feature sizes.³² We surmise that the non-conformal etching is a result of a substantial increase in the concentration of copper ions near the bottom and bottom sidewalls inside the trench or via during the anodic modulation. The size of the interconnect features hinders the diffusion of the copper ions away from the bottom and the collection of copper ions prevents further copper removal at this location. Therefore, we feel that the current flows to more accessible locations (*i.e.* the surface, the re-entrant and sidewalls near the top) and removes copper there. This is similar to what has been described for subconformal filling by P.C. Andricacos, *et al.*,⁹ only applied to the removal of copper instead of the deposition of copper.

Experimental

Patterned wafers containing features ranging from 0.25 to 10.0 μm (~10 to 400 $\mu\text{-in.}$) with an initial copper seed layer were used for the experiments. The 200-mm (7.87-in.) wafer shown in Fig. 6 was sectioned into 19 x 19 mm (0.75 x 0.75 in.) coupons for plating. The anode was a piece of dimensionally stable titanium mesh coated with iridium oxide. The wafer coupons were plated using a rotating disc electrode (RDE) assembly. The rotation speed of the coupon was 400 rpm during the electrically-mediated metallization process and 800 rpm during the anodic etching process. Copper was deposited from a plating bath containing 0.25M copper sulfate, 10 vol% sulfuric acid, 100 ppm polyethylene glycol (PEG) and 50 ppm chloride, at an average current density of 30 mA/cm² (27.9 A/ft²). The plating solution flow rate was 1.0 L/min (0.26 gal/min). The deposition time was 4.0 min. The frequency and the duty cycle were 9000 Hz and 45% cathodic/55% anodic respectively ($i_c = 250$ mA, $i_a = 150$ mA). A DC etch period and an electrically-mediated etch period were investigated at 36 mA and compared with samples plated in the absence of an etch period. The etch time was 30 sec and the frequency for the electrically-mediated waveform was 100 Hz. Schematic diagrams of these waveforms are shown in Fig. 7. Electrically-mediated waveforms can be applied with commercially available pulse power supplies. Metal distribution, filling and planarization of the microscopic features were analyzed using a focused ion beam scanning electron microscope (FIB-SEM).

Results

Figure 8 shows the FIB-SEM cross-section results of copper plating a 0.5- μm (~20- $\mu\text{-in.}$) line with the electrically-mediated waveform in the absence of an anodic etching period. The picture shows that the chosen waveform was capable of filling the line and achieving a planar surface without inducing voids or seams. However, a substantial amount of copper is also present as overfill on the surface of the wafer coupon. Based on this result, it was determined that an additional anodic modulation was necessary to minimize the amount of copper plated on the surface of the samples.

Figure 9 is a comparison between an 8- μm (315- $\mu\text{-in.}$) trench plated with the electrically-mediated waveform in the absence of an anodic etch period and an 8- μm (315- $\mu\text{-in.}$) trench plated with the electrically-mediated waveform followed by an anodic etch period. In both cases, the trenches were not completely filled with copper, indicating that the waveform used to fill the features with copper was not optimized for these features. However, the results in the picture on the right show the feasibility of minimizing the copper plated on the surface of the wafer using the anodic etch period and in this case, all of the copper, including the seed layer that was removed from the surface of the wafer. This result suggests that with further optimization, it may be possible to minimize or eliminate the CMP process.

Figure 10 shows cross sections of trenches and vias ranging in size from 0.25 to 10 μm (~10 to 400 $\mu\text{-in.}$) that were filled with copper using the electrically-mediated waveform followed by an electrically-mediated etching period. The results show the feasibility of using one set of waveform parameters to fill multiple feature sizes in one electrically-mediated ECD step without changing plating baths or masking previously plated features. Complete metallization was achieved for the 0.25 and 0.77- μm (~10 and 30 $\mu\text{-in.}$) features (Figs. 10a and 10b). However, the 0.5- μm (~20- $\mu\text{-in.}$) holes were slightly over-etched as seen in Fig. 10a. Figure 10d shows that the 10- μm (~400- $\mu\text{-in.}$) feature did not fill with the applied waveform. This emphasizes the point that one waveform is not capable of filling different feature sizes, and electrically-mediated waveforms must be tailored to the specific features they are intended to fill. Filling of the 10- μm (~400- $\mu\text{-in.}$) feature could be achieved by optimizing the waveform parameter for this particular feature and then sequencing this waveform with the waveform used to fill the other features present on the wafer.

Electrically-mediated metallization using the proposed micro-profile waveform followed by an anodic etching waveform reduced

the overflow on the surface of the wafer to approximately 1/8 of the overflow observed for chemically mediated processes using two-component copper plating baths. Consequently, the reduction in CMP process waste was approximately 87%. Based on these results, the CMP waste from a 200-mm (7.87-in.) wafer would be reduced from 30 to 50 L (4.0 to 6.7 gal) to the 5 to 7 L (0.67 to 0.93 gal) range.

Figure 11 shows the results of a DC etch at 36 mA versus an electrically-mediated etch at an average current of 36 mA. The electrically-mediated waveform parameters used for deposition of copper prior to etching were identical in both experiments. Therefore it is assumed that the features were filled to the same extent before the etch period was initiated. In both cases, a fairly planar surface was achieved after etching. The 0.77- μm ($\sim 30\text{-}\mu\text{-in.}$) line etched with the electrically-mediated period shown at the right of Fig. 11 exhibits substantially less overflow as compared to the 0.77- μm ($\sim 30\text{-}\mu\text{-in.}$) line etched by DC (Fig. 11, left) indicating the electrically-mediated etch was more efficient at removing the copper than the DC etch period.

Summary

A novel ECD filling profile based on electrically-mediated waveforms is presented for metallization and planarization of interconnect features without defects, such as voids and seams. Compared to traditional filling profiles that utilize two-component copper plating baths containing "difficult-to-control" accelerators,^{9,33} our filling profile suggests defect-free filling of features can be achieved with substantially less overflow. Minimizing the overflow of copper on the surface of the wafer would reduce time and cost associated with the post-deposition CMP process.

The work presented here shows the feasibility of the electrically-mediated process to fill multiple feature sizes on a wafer from a copper plating bath containing only the suppressors PEG and chloride. The absence of difficult-to-control additives, *i.e.*, accelerators and levelers, minimizes process control issues and prevents their incorporation into the copper deposit, which can diminish device performance. Additionally, the work presented shows the feasibility of minimizing copper plated at the surface of the wafer using a short electrically-mediated etch period instead of utilizing three-component copper plating baths that contain "difficult-to-control" levelers to minimize the copper overflow. Once waveform parameters are established for specific feature dimensions, they can be sequenced together to fill multiple features in a single processing step.

Acknowledgment

The authors would like to acknowledge that this material is based upon work supported by the National Science Foundation under Grant No. DMI0131791. The authors would also like to thank Dynatronix Corporation for use of the pulse power supply.^{***}

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Acknowledgments

The author is pleased to acknowledge Dr. Howard A. Kuhn, Dr. Eric W. Brooman and Dr. Donald J. Walukas for their encouragement and support.

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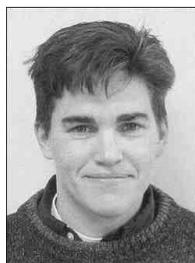
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