PWB Requirements for Increasing Interconnect Density

James P. Langan

Abstract

The high interconnect density pre-required to maximize benefits of recent advances in semiconductor technology imposes changes in PWB fabrication. To accommodate processing speeds > 100MHz and I/O counts > 500, enabler ingredients are expedient viz., surface finishes compatible with advanced bonding techniques; dielectric material with superior electrical, thermal, chemical, and mechanical properties; production procedures for multiplayer boards with micro, buried, and blind vias.. Outlined are avant garde construction methods, materials and processing techniques currently in production or under development to contribute cost-effective approaches for increasing interconnection density.

Surface Finish Issues

For the past 30 years the most preferred PWB surface finish has been fused tin/lead. Reflowed solder plate was first used until the need for solder mask to be applied over copper for optimum reliability initiated a switch to hot air solder leveling. HASL has been the preferred surface finish as solderability is assured when the coating meets thickness specification, has no visible evidence of de-wetting, and displays a bright, shiny appearance.

Limitations of HASL causing PCB manufacturers to contemplate other surface finishes are planarity concerns and compatibility with new bonding techniques. The fabrication industry is familiar with OSP's and nickel/gold electroplating. However, other finishes under consideration require a learning process to achieve maximum functionality. Rapidly gaining acceptance is electroless nickel/gold. This method mandates stringent control to maintain solderability and bondability.

Other techniques with potential to provide planarity and remain compatible with the bonding process are: electroplated Ni/Pd, Pd, immersion tin and immersion silver. These prescribe non conventional procedures, a learning curve, and scrupulous control to guarantee dependability.

Flat fused solder (SSD) provides planarity and a precise volume of solder for attachment of ultra-fine pitch components but assumes special equipment and precise photoimaging . SSD's have the potential to solve some of the fine pitch attachment shortcomings if indeed cost can be controlled.

Design for manufacturability implies a synergistic approach involving teamwork among engineers in design, assembly, and PWB fabrication. The importance of first pass yields dramatically increases as design, materials, and techniques are upgraded to aggrandize the benefits of recent advances in semiconductor technology.

Presently no HASL replacement has the confidence of assemblers accustomed to solderability assurance when the coating meets thickness specification, has no visible evidence of dewetting and is bright and shiny.

The cost differential of the various surface finishes pre-required to achieve the planarity, solderability and bondability of HDI is not as significant as the projected upgrade in material and construction modes. Selection of the surface finish for a particular application must entail design, cost, reliability, and manufacturability issues.

In 1996, HASL was employed 73% of the printed circuit boards produced in North America. The following year HASL accounted for only 60% with a significant increase in coatings that satisfied the planarity concerns with ulra-fine pitch components and new bonding methods from 23% to 35%.

However, this was not maintained in 1998 as alternatives accounted for only 29.5%. The most likely explanation of this is that assemblers experienced a decrease in first pass yields in applications using "No Clean" fluxes and thus limited OSP's to applications

were essential for placement of ultra-fine pitch components.
(See Table I, TMRC Data on Surface Finishes, 1994 – 1999)

To recap: With 1997 data finalized, an increase in 1998 of OSP's was projected. Upon prediction failure, the ensuing 1999 estimate was more conservative.

It should be noted that alternatives to HASL such as immersion tin, immersion silver, Ni/Pd, and flat tin/lead (SSD's) that are presently under evaluation have yet to gain appreciable share of the market.

These finishes have certain advantages for specific applications including:

* Ni/Pd finishes can function as a contact surface and are wire bondably (whereas a soft gold is required for wire bonding and a hard gold for contact.).

* Immersion silver and immersion tin are reported to be less fragile than OSP's and better suited for visual inspection.

* SSD's are ideal for TAB bonding of ultra-fine pitch components.

These approaches are in limited production and with improvement of process controls, anticipatory utilization is projected for applications requiring their specific technical advantage.

Laminate Technology Issues

Presently the most widely used laminate material in the printed circuit board industry is known as FR-4 type, i.e., Epoxy/E glass. Cost effectiveness and ability to satisfy electrical/chemical exactions of most applications account for its popularity.

Co-instantaneously, the exigency for miniaturization and faster process speeds will proliferate use of new material with properties unapproachable via epoxy/E glass.

The mechanical strength of fibers is utilized to provide the structure of copper-clad laminates. Traditionally, this structure has been woven E-glass fabrics of various weave styles and filament diameters. During the past 25 years, both epoxy resins and woven glass cloth have undergone substantial improvements to accommodate precisionistic applications in the electronic industry.

Surface mount technology dictated improvements in bow/twist dimensional stability and thermal resistance (higher Tg) . The increased layers imperative for higher circuit density in multi-layer boards also impose pressures on dimensional stability, Z-axis expansion, and thickness tolerance.

Standard FR-4 materials have a glass transition temperature between 115 – 130 C. By blending multifunctional and tetra-functional epoxies, laminate suppliers have been able to produce mid range (Tg 130 – 150 C) and high (Tg 170 C) epoxies.

Advantages of Multifunctional and Tetra-functional Epoxies:

* Superior performance through multiple thermal excursions

* Reduction in heat damage to plated through hole area, such as barrel

cracking and inner plane separation related to Z-axis expansion

* Improved moisture and chemical resistance resulting in less outgassing defects

* Improved peel strength at higher temperatures since laminate does not soften at lower temperatures

Future Needs in Laminate Technology

The use of advanced laminate material with higher performance properties than multifunctional epoxy will accelerate. In order to remain competitive, faster processing and greater signal integrity will be obligatory for future electronic products.

To obtain these properties, enhancement in both the carrier and resin systems need be employed. The carrier material provides the structure for copper clad laminates by utilizing the mechanical strength of fibers.

Resins provide the bond between the copper and the substrate in multiplayer PWB's and have a strong influence on final electrical/mechanical/ physical properties.

Traditionally this structure has been achieved with woven E-glass fabrics of various weave styles and filament diameters. Also on the horizon are single-ply E-glass fabrics. Fabricators have capitalized on this material for cost efficiency and production of multilayers with thinner dielectrics and more consistent dimensional stability.

Non woven aramid random fiber material has the unique property of lower density (15% lighter than conventional boards) and the propensity of micro-via generation by either plasma or laser.

To satisfy future needs, PWB laminate material must provide higher thermal stability vis-à-vis glass transition temperature > 170 C, lower thermal expansion x-y CTE >9pmm/ C, and a lower dielectric constant. (1)

(cf Table II for cost and application information on advanced resin systems.)

Micro-via/Buildup Technology

Standard drilling technology can facilitate a via pad size of 635 microns (25mil) with a 381 micron (15mil) hole. Cost rises significantly as smaller hole size is exacted. A via of 203 microns (8mil) appears to be the practical limit but even that level may augment a PWB price as high as 30%. Also, as the hole size gets smaller for the same thickness board, the aspect ratio increases. High aspect ratio holes tend to decrease reliability due to plating and solder fill problems.

To form a small via methods other than mechanical drilling are employed, viz., laser, plasma, photochemical. This has led to a new approach to multi-layer manufacturing, i.e., "build up technology". Modi operandi are in production or under scrutiny to determine the most operative and reliable manner to effect thinner multi-layer PWB's with buried and blind micro vias and narrower lines/spaces. (2) (See Table III)

References:

(1) IPC, Technical Marketing Research Council Reports (1995 – 1999)

(2) Coombs, Clyde F., "Printed Circuit Handbook", McGraw Hill Inc., New York, 4th Eition 1996, Ch. 9.51
d

(3) Dwyer, Herbert E., "Advanced Electronic Interconnect – Cost and Opportunities", Proceedings Nepcon West, March, 1998

Table I

Surface Finishes
(TRMC Data) (1)

	1994	1995	1996	1997	1998	1999*
HASL	71.5%	75.3%	72.9%	59.7%	67.8%	67.0%
Sn/Pb Reflowed	10.0%	5.2%	4.1%	5.0%	2.7%	1.4%
OSP's	12.7%	15.9%	17.3%	28.2%	19.2%	21.4%
Ni/Au	3.8%	1.5%	2.0%	5.8%	8.3%	8.0%
Other	2.0%	2.1%	3.7%	1.3%	2.0%	2.2%
	100%	100%	100%	100%	100%	100%

Table II

Cost and Application Information on Advanced Resin Systems (2)

Application	Resin	Tg	Cost*
High volume – medium & high Technology – low cost PCMCIA	Multifunctional Epoxy	140 C	1.0
Thick M/L, back-planes, DCA, BGA, under-hood, PCMCIA, PGA	Multifunctional Epoxy	170 C	1.3
MCM-L, CA, BGA, high speed computing, PGA	BT/Epoxy	180 C	1.5
Military hardware	Polyimide	260 C	2.3
High reliability avionics	Toughened Polyimide	220 C	2.4
Controlled MCM-Ls, laser micro-via MCM-Ls, PCMCIA	Thermount Polyimide	220 C	2.4
High speed computing telecommunications hardware, high frequency electronics, high reliability	Cyanate ester	250 C	2.6

*** 1.0 Based on a 6 layer multifunctional epoxy material Tg 140 C**

Table III

Micro-via/Build-up Technologies

Technology	Insulating Material	Lines/Spaces Microns (Mils)	Via/land Dia. Microns (Mils)
Microfilled vias (MfVia)	Epoxy, PID, 3.8	75/75 (3/3)	125/250 (5/10)
Photo-via Redistribution layer	Epoxy, PID	100/100 (5/5)	125/380 (5/15)
Conductive adhesive bonded flex	Polyimide film 3.8	25/50 (1/2)	25/200 (1/8)
Seq. bonded film (DYCOstrate)	Polyimide film 3.8	75/75 (3/3)	100/250 (4/10)
Surface laminar circuits (SLC)	Epoxy, PID, 3.8	75/75 (3/3)	125/250 (5/10)
Build-up structure systems (IBSS)	Epoxy + PES, 3.8	75/75 (3/3)	125/250 (5/10)
Carrier formed circuits	Epoxy acrylate, 3.8	100/100 (4/4)	150/400(6/16)
Roll sheet build-	Epoxy, 3.2	100/100 (4/4)	150/450(6/18)
Sheet build-up	Epoxy, 3.2	75/75 (3/3)	100/400(4/16)
Sequential bonded solid vias	Epoxy aramid, 3.8	100/100(4/4)	125/250(5/10)
High density inter-connect (HDI)	Polyimide film, 3.8	25/50 (1/2)	25/200(1/8)
Buried bump inter-connect	Epoxy glass, 4.3	100/100(4/4)	125/250(5/10)
Micro-wiring	Polyimide film, 3.8	100/100(4/4)	125/250(5/10)
Conductive ink	Epoxy, PID, 3.8	75/75(3/3)	125/1`25(5/5)