Electrically Mediated Metallization of Printed Wiring Board and VLSI Features

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ABSTRACT

This paper describes an electrically mediated metallization process for manufacturing of printed wiring boards and VLSI features on wafers. In contrast to traditional chemical mediation of metallization processes, the electrically mediated process does not rely on difficult to control leveling additives such as brighteners and/or levelers. The methodology for selection of the electrically mediated process parameters is based on considerations of hydrodynamics and microprofiles and macroprofiles on the metal distribution. The feasibility of the electrically mediated process has been demonstrated at the prototype scale. Results from laboratory and prototype facilities and initial data from a PWB facility will be discussed.

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Introduction

The continuing trend towards miniaturization of consumer electronics is placing considerable technological challenges to all segments of the electronics industry. Specifically, in advanced integrated circuits (ICs), copper interconnections are replacing aluminum.[1,2] Since the performance capabilities and miniaturization of IC devices are proceeding at a rate significantly faster than the printed wiring board technology required to interconnect them,[3] the need for chip scale packages (CSPs) and high density interconnect printed wiring boards (HDI-PWBs) has emerged. As depicted in Figure 1, the CSP and HDI-PWB provide the z-axis interconnection between the IC and the PWB.

The challenge of plating electronic interconnects and VLSI features on ICs is one of leveling, *i.e.* the uniform deposition of a conductor into microprofiles.[4] There are two types of leveling; geometric leveling and true leveling.

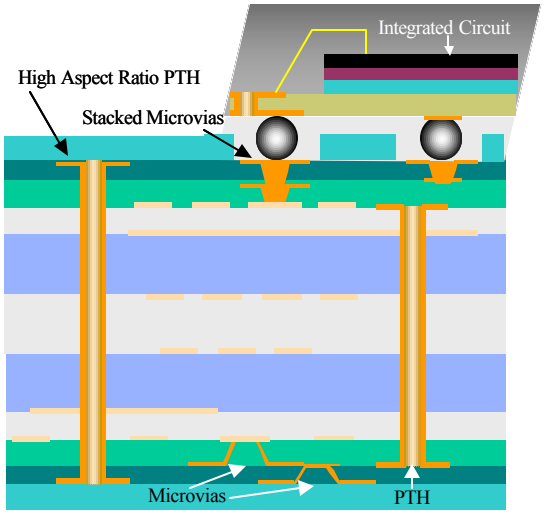

Figure 1 - Schematic of Advanced Electronic Package.

Geometric leveling results from a uniform or primary current distribution; consequently the plating rate must be very slow. Geometric leveling only occurs when the deposit is at least as thick as the depth of the microprofile; consequently the overplate is considerable. Geometric leveling is impractical for fabrication of electronic interconnects and VLSI features.

True leveling results from the preferential adsorption of a specific leveling additive or additives on the high current density peaks or corners of the microprofile. True leveling requires precise control of these additives; also known as levelers and brighteners.

In conventional direct current (DC) plating of plated through holes (PTHs) for the PWB industry, leveling additives are incorporated in the plating bath to improve the throwing power and to yield a fine-grained deposit.[5,6] However, considerable challenges exist for extension or insertion of PTH electroplating processes to the smaller microvias and IC features. Specifically, the proprietary chemistries used in "conventional" and "high throw" baths do not necessarily provide acceptable results for smaller interconnect features[7] and proprietary chemical formulations must be optimized for different feature sizes.[8] Furthermore, bath maintenance and control issues associated with the leveling additives are exacerbated at HDI, CSP and IC feature sizes.

To meet the plating challenge of advanced electronic interconnects, non-DC plating processes have recently received considerable interest[9,10,11,12,13]. While these non-DC processes have been referred to by a variety of names, *e.g.* periodic reverse plating and pulse reverse plating, they all utilize brighteners and/or levelers and are therefore a form of true leveling. Consequently, the challenge of precise control of leveling additives remains.

Recently, copper plating for electronic applications, **without brighteners and levelers**, has been reported[14,15,16,17].

This process is termed electrically mediated copper plating in contrast to the conventional chemically mediated approach using leveling additives. Below we present further results using electrically mediated copper plating of electronic interconnects[18,19] and VLSI features[20].

Approach

In the electrically mediated approach, the forward on-time/peak current and reverse on-time/peak current are tuned to plate specific electronic features. The rationale basis for selecting the process parameters includes considerations of microprofiles and macroprofiles as a function of feature size and aspect ratio. This approach is in contrast to previous studies[9,10,11,12,13], which utilized a waveform consisting of a long forward pulse followed by a short reverse pulse in the presence of leveling additives. As suggested from fundamental considerations,[21] changes in waveform parameters should have a substantial impact on copper plating of sub-micron features.

While the detailed rationale for selection of waveform parameters was presented previously[14,15,16], the general findings are that there are specific process parameters for specific electronic features. For example, PTHs require a relatively long forward on-time followed by a relatively short reverse on-time. The sum of the forward on-time and reverse on-time, as well as any off-times, is approximately 10 to 20 msec, or 50 to 100 Hz. The general form of the electrically mediated process waveform for PTHs is presented in Figure 2.

For high aspect ratio PTHs, microvias, *i.e.* features less than 150 µm, and IC features, the electrically mediated process parameters consist of a relatively short forward on-time/high forward peak current followed by a relatively long reverse on-time/low reverse peak current. For high aspect ratio PTHs and microvias, the sum of the forward on-time and reverse on-time, as well as any off-times, is approximately 1 to 2 msec, or 500 to 1000 Hz. For IC features, the sum of the forward on-time and reverse on-time as well as any off-times, is approximately 0.2 to 0.5 msec, or 2000 to 5000 Hz. The general form of the electrically mediated process waveforms for high aspect PTHs/microvias and IC features are presented in Figure 3 and 4, respectively.

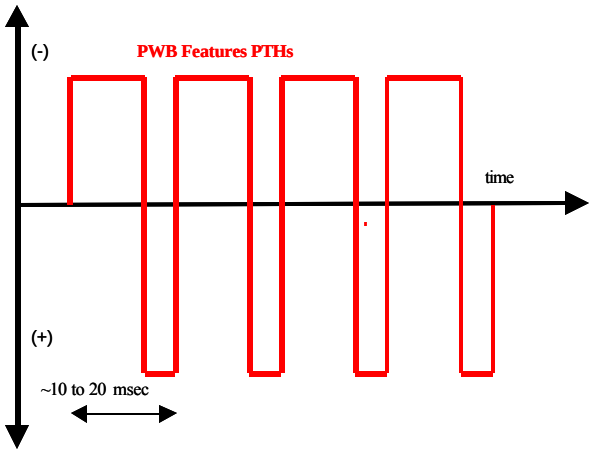

Figure 2 - Generalized Waveform for PTH.

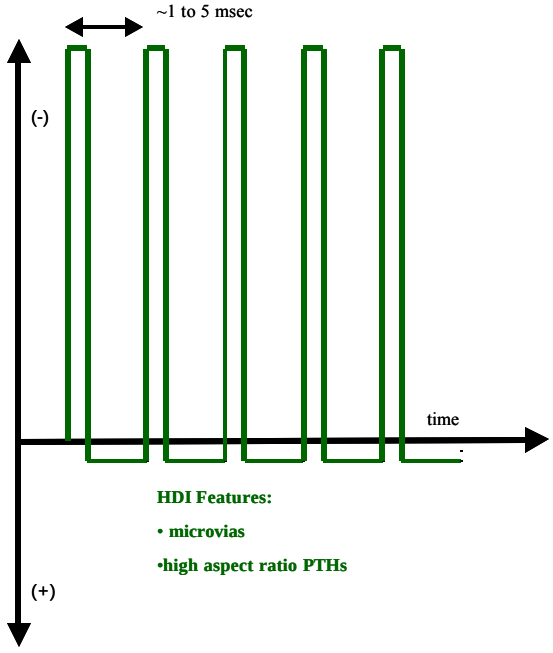

Figure 3 - Generalized Waveform for High Aspect Ratio PTHs and Microvias.

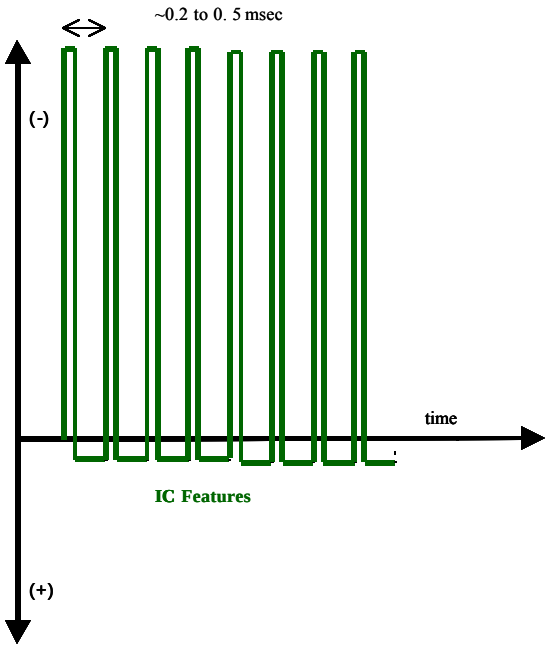

Figure 4 - Generalized Waveform for IC Features.

Experimental

An acid copper sulfate solution containing 60 g/L $CuSO_4$, 9% by volume of H_2SO_4, 60 ppm Cl^-, and 350 ppm PEG was used as the copper electroplating bath for all experiments. The plating bath temperature was 25 ^oC.

For the HDI-PWB features, plating experiments were conducted on 8 □x18□ panels of 0.125□ and 0.250□ thicknesses containing microvias, PTHs, BGAs, and IST features. The plating line (vertical) consisted of a single panel flight bar with eductors oriented at 90° perpendicular, knife edge agitation and mesh insoluble anodes. As described previously, the insoluble anodes offer potential advantages for reverse pulse plating[22]. For the CSP and IC features, plating experiments were conducted on 1.9x1.9 cm samples in a rotating electrode apparatus.

Results

A major advantage of the electrically mediated approach is that different sized features, on the same board layer or wafer, can be metallized in one process step, without any change in chemistry. In Figure 5, the results for electrically mediated copper plating of a 50 µm microvia and a 325 µm PTH in one process step, are presented. The waveform sequence used was a short forward on-time/long reverse on-time, at a frequency of approximately 300 Hz, followed by a long forward on-time/short reverse on-time, at a frequency of approximately 50 Hz. Good throwing power was achieved in both features.

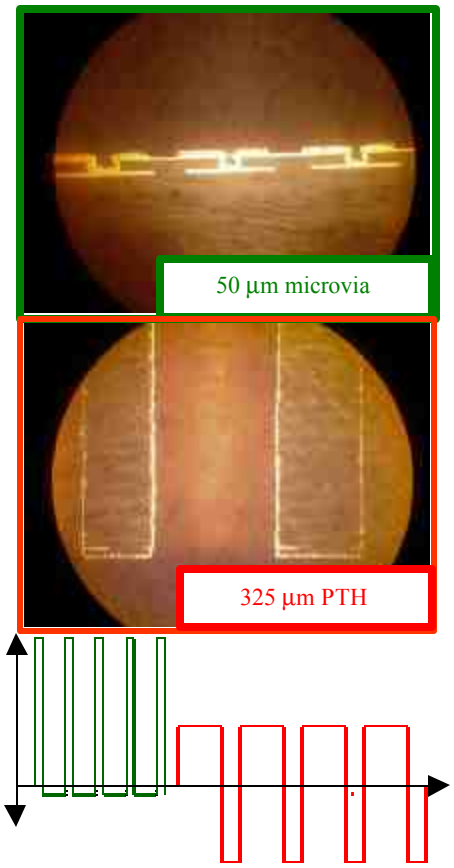

Figure 5 – Metallization of 50 µm microvia and 325 µm PTH, in one process step using waveform sequencing.

Waveform sequencing can also be used for metallization of ultra-high (20:1) aspect ratio PTHs, to address the hydrodynamic inaccessibility of the PTHs. Figure 6 shows a waveform sequence consisting of a long forward on-time/short

reverse on-time, followed by a short forward on-time/long reverse on-time. Using this sequence, a throwing power of 128% was obtained for a PTH with a high aspect ratio of 20:1, and a throwing power of 100% was obtained for a PTH with a low aspect ratio of 4:1.

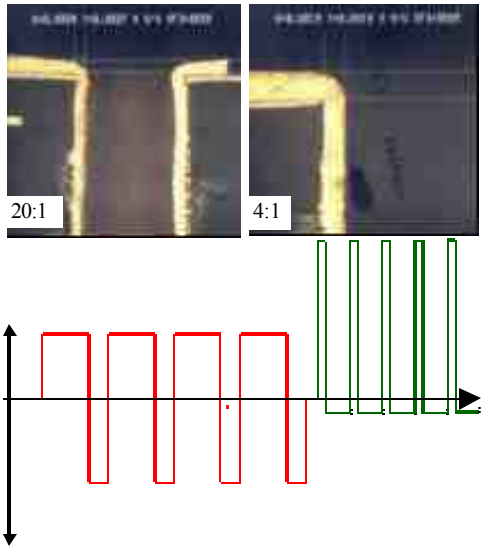

Figure 6 – Metallization of 20:1 and 4:1 PTHs, using waveform sequencing.

Figures 7, 8 and 9 show that electrical mediation can also be applied to metallization of VLSI features on IC's. Excellent, void-free filling for 0.25, 0.5, 0.75 and 1 µm IC features were obtained with minimal overplate, using a waveform sequence consisting of a short forward on-time/long reverse on-time, followed by a short reverse on-time etching step. The minimization of overplate results in a reduction in the amount of chemical mechanical planarization (CMP) required in subsequent processing. Figure 10 shows the reduction in overplate due to the use of electrically mediated etching, as compared to DC etching.

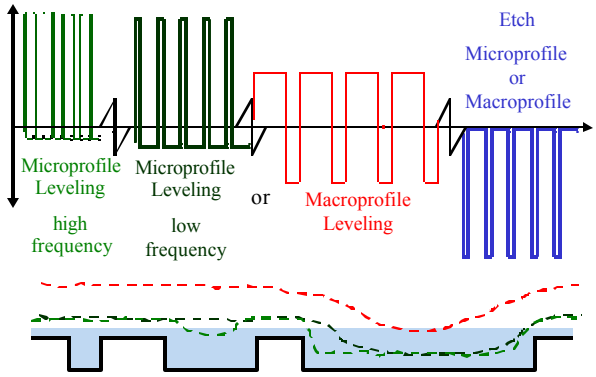

Figure 7 – Variety of electrically mediated processes which can be applied to metallization of VLSI features.

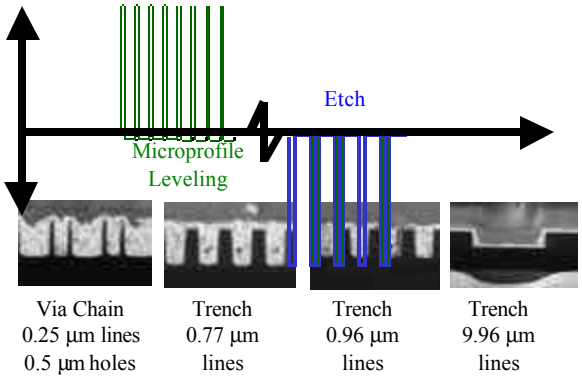

Figure 8 – Metallization of various IC features, using electrical mediation and waveform sequencing.

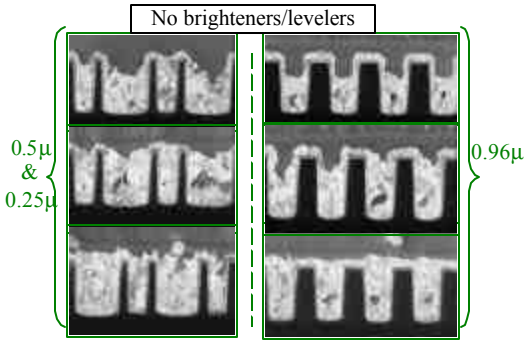

Figure 9 – Metallization of IC features, using electrical mediation, with minimal overplate/CMP.

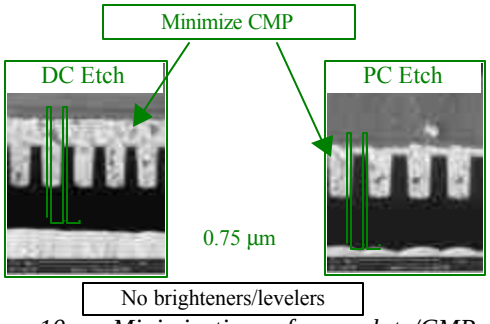

Figure 10 – Minimization of overplate/CMP, by control of etching step.

Summary

An electrically mediated process for copper plating of electronic interconnects and VLSI features is described[23,24]. Specifically, copper plating PTHs and microvias for HDI-PWB, microvias for CSP, and IC features ranging in size from 325, 50, 1, 0.75, 0.5 and 0.25 µm. In contrast to conventional plating art based on leveling additives, the electrically mediated process is based on predictable knowledge. Consequently, as new electronic packages are required, the electrically mediated process parameters are selected from a library of process parameters.

The critical parameters of the electrically mediated process are forward and reverse on-times and forward and reverse peak currents. By understanding the influence of hydrodynamics, macroprofiles and microprofiles on electrodeposition, the process parameters are tuned to the electronic interconnect feature of interest. In this manner, different electronic interconnect and VLSI features may be plated in a single step by sequentially changing the waveform process parameters[25].

Acknowledgement

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