A Low Cost Semiconductor Metallization/Planarization Process

H. Dyar, E.J. Taylor, J. Sun, Maria Inman Faraday Technology Inc., 315 Huls Drive, Clayton, OH 45315

This paper will present an electrically mediated process for copper metallization and planarization of semiconductor scale features. Compared to traditional leveling processes, the proposed electrochemical deposition process does not require the addition of difficult-to-control chemical brighteners and levelers to the plating solution, has high plating rates and substantially reduces waste associated with the deposition process. The process is demonstrated by copper deposition onto 8-inch VLSI wafers. Results such as deposit thickness distribution and uniformity, structure, and grain size, as a function of electrically mediated leveling parameters are presented for feature sizes in the range of 0.25 – 1 μm.

For more information, contact:
Phillip Miller
Faraday Technology, Inc.
315 Huls Drive
Clayton, OH 45315
Phone: (937) 836-7749
Fax: (937) 836-9498
phillipmiller@faradaytechnology.com

Introduction

For the past four decades, the semiconductor industry has continued to improve semiconductor devices in order to comply with the market demand for higher performance, cost-effective products. The continued decrease of feature sizes on integrated circuits (IC) has increased circuit performance and yield at a lower cost per function on chips. According to the Semiconductor Industry Association (SIA), the reduction in feature size is approximately 30% every three years.[1] However, as feature sizes shrink into the submicron region (<0.25 μm), the resistance-capacitance (RC) delay associated with the interconnect features becomes the dominant performance limiting factor. The RC delay results from an increased resistance due to the narrowing of the interconnections and an increased capacitance due to the closer proximity of the interconnections. An increase in the RC delay has a negative impact on the speed and power consumption of IC devices.

Originally metal interconnects on IC devices were fabricated from aluminum and aluminum alloys, since aluminum has a relatively low electrical resistance (~2.7 μΩ cm) and can be easily deposited and etched. However, as feature sizes were reduced, it became apparent that aluminum was unable to reliably conduct the current necessary to maintain or increase IC performance. To compensate for this problem, the semiconductor industry began investigating the use of copper as a replacement for aluminum as the conductor on IC devices, and in 1997 IBM announced the integration of copper chip technology into its products.[2]

The implementation of copper into IC devices has several notable advantages compared to aluminum that makes it attractive for metallization of interconnect features:[3,4,5]

- low electrical resistance
- high electromigration resistance
- high thermal conductivity
- low cost
- high reliability
- proven deposition methods

The electrical resistance of copper (~1.7 μΩ cm) at ambient temperature is approximately 40% lower than aluminum[6,7] and approximately 50% lower than many of the aluminum alloys[4] employed in IC devices. The lower electrical resistance of copper decreases the RC delay and produces higher currents at a given voltage enabling the production of faster, denser chips with increased computing power. In addition, the lower resistivity of copper reduces the necessary number of interconnect levels, which drastically decreases the number of processing steps, thus reducing processing costs.[5]

The switch from aluminum to copper for metallization of interconnect features has also resulted in a decrease in electromigration; a phenomenon identified as one of the primary failure mechanisms limiting IC reliability. Electromigration occurs when mobile electrons responsible for the electrical current within the circuit collide with stationary atoms, causing diffusive transport of these atoms in the direction of the electron flow. As a result, the metal

thins in one area of the interconnect while accumulating in another area, initiating electrical failure of the IC.[4] Copper interconnects have a higher electromigration resistance than those constructed from aluminum and its alloys because copper atoms are heavier and contain stronger metallic bonds. The higher electromigration resistance of copper increases the reliability of the IC for a given interconnect design.

Aluminum interconnects are fabricated by conventional sputter deposition and reactive ion etching (RIE) techniques. Copper is not easily etched by conventional RIE techniques due to the lack of volatile by-products; therefore the aluminum to copper conversion in the semiconductor industry required the development of new methods for depositing copper. Several techniques have been investigated for filling of interconnect features with copper including physical vapor deposition (PVD), chemical vapor deposition (CVD), electroless plating and electrochemical deposition (ECD).[5,8,9,10] The most common technique currently practiced in the semiconductor industry is the Damascene process, which utilizes ECD for depositing the copper onto IC devices.

The Damascene process, developed by IBM, involves etching a pattern of interconnect features, *i.e.* trenches and vias, in a dielectric film, then fills the pattern with copper using ECD techniques. Before depositing the copper, a barrier layer must be applied to prevent the copper from diffusing into and poisoning the dielectric material. Additionally, a small copper seed layer is deposited using a non-electrolytic process, such as PVD, prior to complete filling of the interconnect features with copper using ECD. The seed layer is necessary to ensure good electrical contact to all areas of the wafer where copper deposition is desired during the ECD process. The main problems associated with ECD of copper interconnect features are the filling of submicron, high aspect ratio vias and trenches without void or seam formation and the overfill of copper on the wafer surface.

The formation of voids and seams can occur because the size and geometry of the trenches and vias makes the bottoms of these features less accessible to copper during the seeding and filling process. These defects can ultimately lead to failure of the IC component. To initially avoid defects during the filling process, the seed coverage must be smooth and continuous over the entire feature. Dissolution or oxidation of the seed layer must be avoided during immersion of the wafer into the plating bath, or void formation occurs.[11] Once an optimal seed layer has been deposited, the trench or via can be filled with copper using ECD. Different filling profiles have been described,[6] and superfilling, *i.e.* filling of trenches and vias from the bottom up, is currently the most accepted profile for producing defect-free features.

Superfilling occurs due to increased deposition rates along the sides and bottom of the trenches and vias. This is usually achieved by passing direct current (DC) through a copper plating solution containing proprietary organic additives, such as brighteners and levelers.[6] Although the additives help to eliminate defects in the filling process, they create additional problems. Incorporation of the additives into the copper deposits can increase resistivity.[12] Also, the additives are slowly consumed during the deposition process. Since modeling has shown that the smallest imbalance in the system can create defects in the trenches and vias[13], it is necessary to closely monitor the concentration of the additives. Moreover, different feature sizes require different amounts of chemical additives for defect-free filling of trenches and vias.[14] For these

reasons, it is necessary to develop filling processes that substantially reduce or even eliminate the need for organic additives in plating solutions.

Because the seed layer covers all of the features on the wafer, including the surface, ECD of copper occurs over the entire wafer. Copper deposited on the wafer surface is referred to as overfill. The overfill is typically removed subsequent to ECD of the copper using chemical mechanical planarization (CMP). Typically, anywhere from 0.5 μm to 1.5 mm of copper needs to be removed to leave the planarized trenches and vias embedded in the dielectric material.[15] It is estimated that between 30 to 50 liters of waste slurry are generated per eight-inch wafer during the CMP process.[16] Reducing the overfill on the wafer surface would reduce the polishing time and slurry waste, thus reducing manufacturing costs.

Pulse current (PC) and pulse reverse current (PRC) processes are being investigated as alternatives to the conventional DC processes used for ECD of copper interconnect features.[12,17,18,19,20,21] Compared to DC plating, PC and PRC processes present several potential advantages, such as increased ECD rates, improved deposition properties, higher current efficiency and the reduction of additives.[22,23] In addition, when optimized for specific features, PC and PRC waveforms have the ability to completely fill vias and trenches with substantially less overfill of copper on the surface of the wafer.

Approach

PC and PRC waveforms have the potential to significantly enhance ECD processes by optimizing the associated process parameters, specifically the cathodic (forward) pulse current, i_c, the anodic (reverse) pulse current, i_a, the cathodic on-time, t_c, the anodic on-time, t_a, and the off-time, t_0, shown in Figure 1.

The period, T, of the waveform is the sum of the cathodic and anodic pulse on-times and the off-time and the inverse of the period results in the frequency, f, of the modulation. Additionally, the cathodic duty cycle, γ_c, and the anodic duty cycle, γ_a, are the ratios of the respective pulse on-times to the period. The average current density (i_{avg}) or net ECD rate is given by:

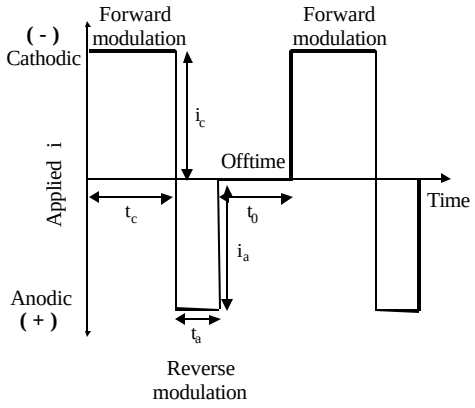


Figure 1- PC and PRC waveform

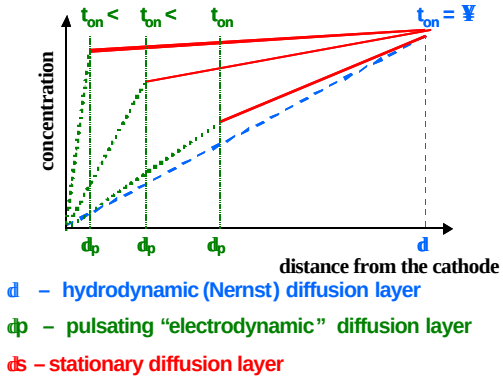


Figure 2- Schematic representation of diffusion layers

$$i_{aver} = i_c\gamma_c - i_a\gamma_a \qquad (1)$$

During ECD processes the current density is limited by the diffusion of the ions to the electrode surface, which is related to the thickness of the diffusion layer. In a DC process, it is the hydrodynamic diffusion layer, δ, that establishes the current density. It has been shown in previous work[24,25,26,27,28] that during PC and PRC processes, a "duplex diffusion layer" is established, incorporating both a stationary layer, δ_s, and a pulsating layer, δ_p (Figure 2) referred to as the "electrodynamic diffusion layer"[29]. Assuming a linear concentration gradient across the electrodynamic diffusion layer, the thickness of δ_p is described by the following equation:[25]

$$\delta_p = (2Dt_{on})^{1/2} \qquad (2)$$

where D is the diffusion coefficient of the reacting species and t_{on} is the pulse on-time.

In order for the electrodynamic diffusion layer to influence the deposition process, the mass transport effects must be significant during the pulse on-time. This occurs when the reacting species at the electrode/solution interface is exhausted and must be replenished by ions diffusing to the electrode. The time it

takes for the reacting species to be depleted at the interface is referred to as the transition time, τ, and is defined by Equation (3):

$$\hat{o} = \frac{(nF)^2 C_b D}{2i_c^2} \qquad (3)$$

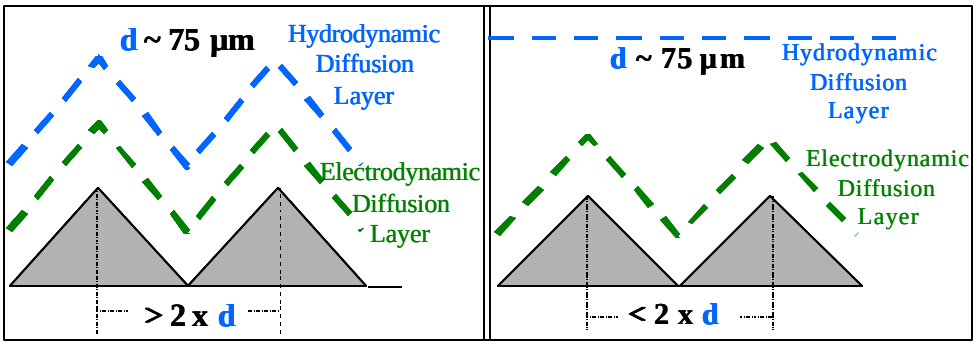


Figure 3- (left) Macroprofile; (right) Microprofile

where n is the number of electrons transferred, F is Faraday's constant and C_b is the bulk concentration of the ions being deposited. Therefore, mass transport effects only strongly influence the electrochemical deposition process when t_{on} is much larger than τ.

The influence of mass transport effects on the ECD process produces two different situations. The first situation, shown at the top of Figure 3, is referred to as a macroprofile case. In a macroprofile, the surface roughness is large compared to the thickness of the diffusion layer, and the diffusion layer tends to follow the surface contour. Under mass transport or diffusion control, a macroprofile results in a uniform current distribution and a conformal deposit or etch, depending on whether a forward or reverse pulse is applied during the ECD process.

In the second situation, the surface roughness is small compared with the thickness of the diffusion layer. This results in a microprofile case shown at the bottom of Figure 3. Under mass transport control, a microprofile results in a non-uniform current distribution and preferential deposition or etching during the ECD process.

For void-free copper deposition into trenches and vias, the optimum waveform should uniformly deposit copper during the cathodic modulation. Since the thickness of the diffusion layer under conditions of moderate bath agitation is on the order of 75 µm, and the vias and trenches are less than 1 µm, the filling of the trenches and vias fits a microprofile case. To ensure uniform deposition of the copper into the trenches and vias, the waveform parameters should be chosen so the microprofile is converted into a macroprofile during the cathodic modulation. This can be achieved by using a high cathodic peak current for a relatively short on-time. These parameters can be rationalized by examining Equation (2) and Equation (3). To convert from a microprofile to a macroprofile, the diffusion layer thickness must be decreased. According to Equation (2), the diffusion layer is proportional to the on-time, so a short on-time will produce a small diffusion layer. Also, for mass transport effects to be significant, the transition time, τ, must be much smaller than the on-time, t_c. Equation (3) shows that the transition time is inversely proportional to the cathodic peak current, so a large cathodic peak current will yield a short transition time. In the case of a macroprofile, copper deposition will be conformal, however, conformal filling profiles often produce seams in trenches and vias and result in significant overfill as shown in Figure 4.

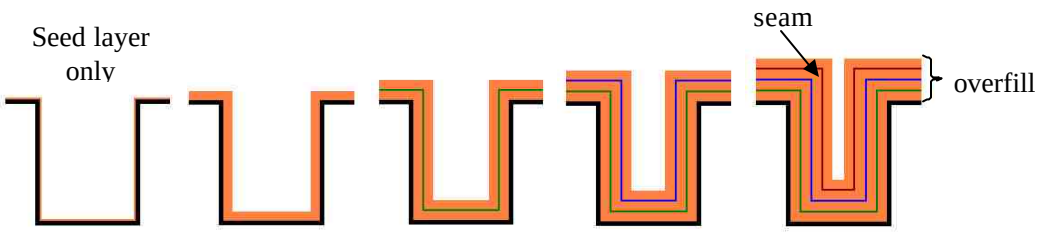


Figure 4 – Conformal filling profile during PC process

Using a PRC process instead of a PC process reduces overfill and eliminates defects by conformally depositing copper during the cathodic modulation and preferentially etching copper from the surface, re-entrant and upper sidewalls of the trenches and vias during the anodic modulation. This is achieved by using the high cathodic peak current for a short on-time during deposition, then creating a non-uniform current distribution during the etch process using a low anodic peak current for a relatively long on-time. Again, the choice of these parameters can be justified with Equation (2) and Equation (3). An additional anodic modulation may be added to further reduce overfill and electrochemically level the surface of the feature.

Electric field effects cannot be responsible for the uneven current distribution that leads to the non-conformal etching of the vias and trenches since the ohmic drop in the plating solution is negligible at the scale of the feature sizes. The non-conformal etching is a result of a substantial increase in the concentration of copper ions near the bottom and bottom sidewalls inside the trench or via. The size of the interconnect features hinder the diffusion of the copper ions away from the bottom and the collection of copper ions prevents further copper removal at this location. Therefore, it is thought that the current flows to more accessible locations (*i.e.* the surface, the re-entrant and sidewalls near the top), and removes copper there. This is similar but opposite in nature to what has been described for subconformal filling by P.C. Andricacos[6]. A schematic of the proposed filling profile and an example of the waveform is shown in Figure 5. The filling profile begins by showing the interconnect feature prior to ECD, containing only the seed layer. This is followed by the first deposition process, the schematic of where the etching will occur, then the feature after etching. The final result of this filling profile is a defect-free copper filled trench or via featuring considerably less overfill compared to trenches and vias filled under conformal or superfilling profiles. Also, the etching and leveling processes planarize the surface of the feature. In superfilling, although it is considered defect-free, the formation of a dimple above the filled trench or via commonly occurs as shown in Figure 6. The non-planar surface must be planarized by a post-deposition CMP process. An uneven distribution of copper causes a rough surface, which reduces the effectiveness of CMP and diminishes the performance of the device.

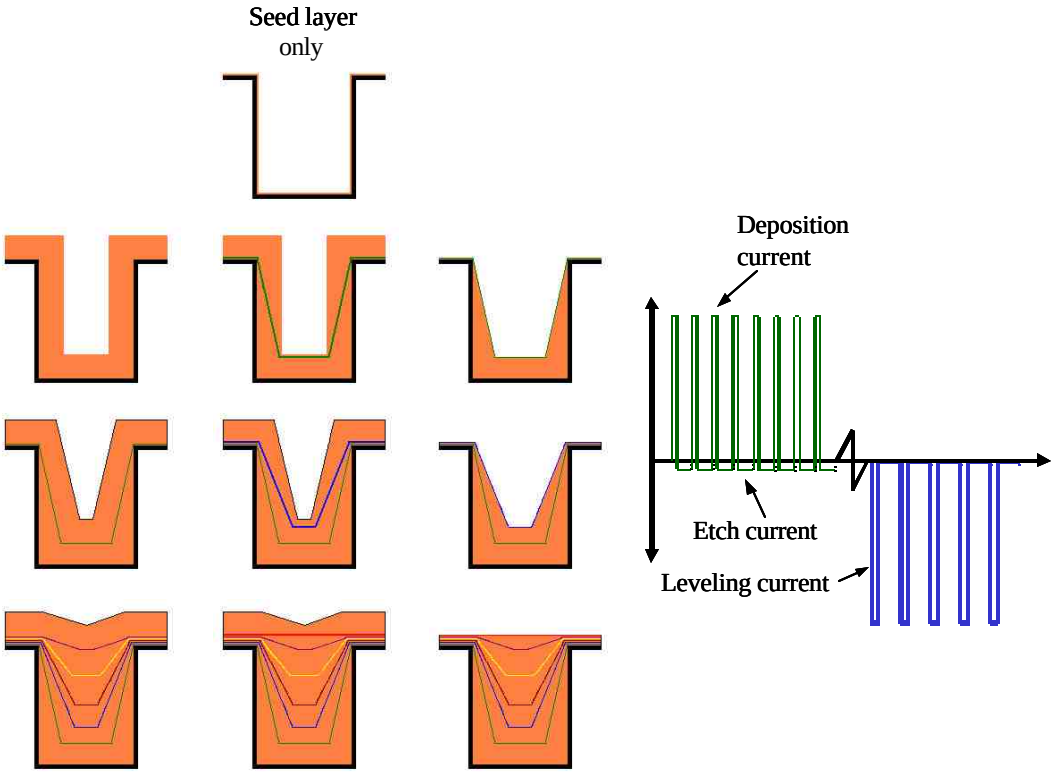


Figure 5 - Novel filling profile for PRC process (left); Example of PRC waveform (right)

Experimental

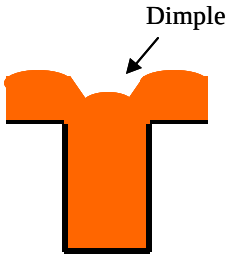


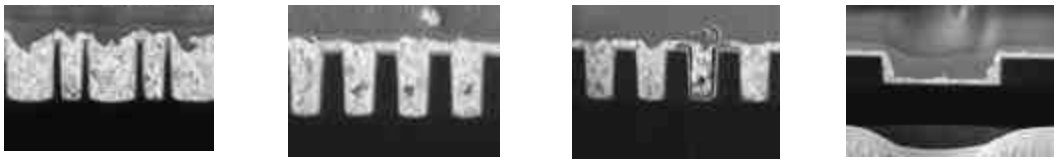
Figure 6 – Interconnect feature illustrating dimple effect

An acidic copper sulfate ECD electrolyte bath comprised of 60-65 g/L $CuSO_4 \cdot 5H_2O$, 1.8 M H_2SO_4, ~300 ppm polyethylene glycol (PEG) and ~60 ppm chloride ion, was used for experiments. The PEG acts as an inhibitor in the deposition process, and is not considered a difficult-to-control additive since its concentration can be increased well beyond the optimal level without effecting the filling of interconnect features.[11] Wafer samples of 25 x 25 mm (1" x 1") were used in conjunction with a rotating disk electrode assembly system. The cathode was rotated at speeds between 400 and 800 rpm. A piece of coated titanium mesh was used as the anode. Frequencies of 100 to 6000 Hz were investigated. Plating times varied from 1 to 4 minutes and leveling times were varied between 0.5 and 1 minute. Average current densities between 10 and 30 mA cm^{-2} were examined. A Dynatronix Pulse Power Supply, model PCT-8023, has been chosen for application and control of the waveform parameters because of its

compatibility with semiconductor assembly processes. Metal distribution and filling of the features was analyzed using FIB-SEM.

Results

Figure 7 shows work previously done in the lab. Cross sections of copper filled trenches and vias ranging in size from 0.25 to ~10 µm were filled using a



(a) Via Chain
0.25 µm lines
0.5 µm holes

(b) Trench
0.77 µm lines

(c) Trench
0.96 µm lines

(d) Trench
9.96 µm lines

Figure 7 – SEM of trenches and vias filled using a PRC waveform similar to the example shown in Figure 5.

PRC waveform similar to the one presented in Figure 5. Figure 7a shows that by optimizing waveform parameters, it is possible to fill multiple feature sizes in one ECD step. One set of waveform parameters was used for simultaneously filling the features ranging in size from 0.25-10 µm. Complete metallization was achieved for the 0.25 and 0.77 µm features (Figure 7a and 7b) with minimal overfill. The overfill was approximately 1/8 the overfill typically observed for vias and trenches filled by the superfilling profile. The 0.5 µm holes filled but were slightly over-etched. The 10 µm feature was not filled. This emphasizes the fact that different feature sizes require the use of different waveforms and PRC waveforms must be tailored to the specific features they are intended to fill. Once the waveform parameters have been determined for each feature size, they can be sequenced together to achieve copper filling of all features in the same processing step. Further investigation into waveform sequencing is underway.

In addition to a cathodic deposition current and an anodic etch current, the proposed PRC waveform shown in Figure 8 includes a DC initiation current before the PRC process begins. As feature sizes decrease, a continuous and uniform seed layer becomes increasingly important if the formation of defects is to be avoided. The initiation current provides cathodic protection of the seed by having the current flowing when the wafer makes initial contact with

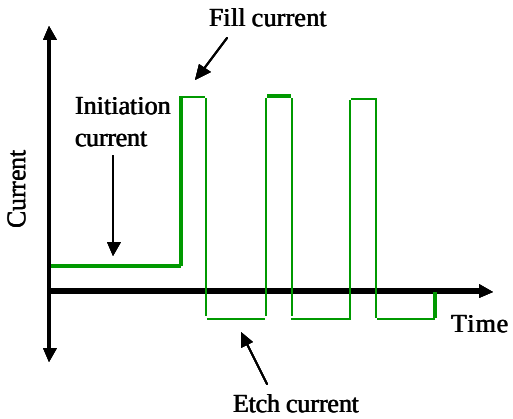


Figure 8 – PRC waveform including DC initiation current for cathodic protection of the seed layer

the ECD electrolyte bath. Cathodic protection, or 'hot entry', aids in preventing dissolution or oxidation of the seed layer, which can cause the formation of defects. Moreover, a small initiation current yields a slow, conformal deposition of copper that promotes continuity and thickening of the seed layer before the primary filling process occurs. Further investigation into the use of cathodic protection with and without the use of accelerating chemistries in the ECD electrolyte bath was being investigated at the time of preparing this paper.

Summary

A novel ECD filling profile for PRC waveforms, based on concentration polarization during the anodic etching period, is presented for metallization and planarization of interconnect features without defects, such as voids and seams. Compared to traditional filling profiles described in the literature,[6,30] our filling profile suggests defect-free filling of features with substantially less overfill. Minimizing the overfill reduces time and cost associated with the post deposition CMP process.

Work presented indicates that by optimizing waveform parameters, specifically the forward and reverse peak currents and the forward and reverse on-times, the distribution and uniformity of the deposit can be controlled and multiple features can be simultaneously filled, thus reducing associated manufacturing costs. Additionally, it is believed that cathodic protection of the seed layer will further improve the metallization process. New waveforms that include a cathodic protection initiation current are currently being investigated. Once waveform parameters are established for specific feature dimensions, they will be sequenced together to fill multiple features in a single processing step.

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